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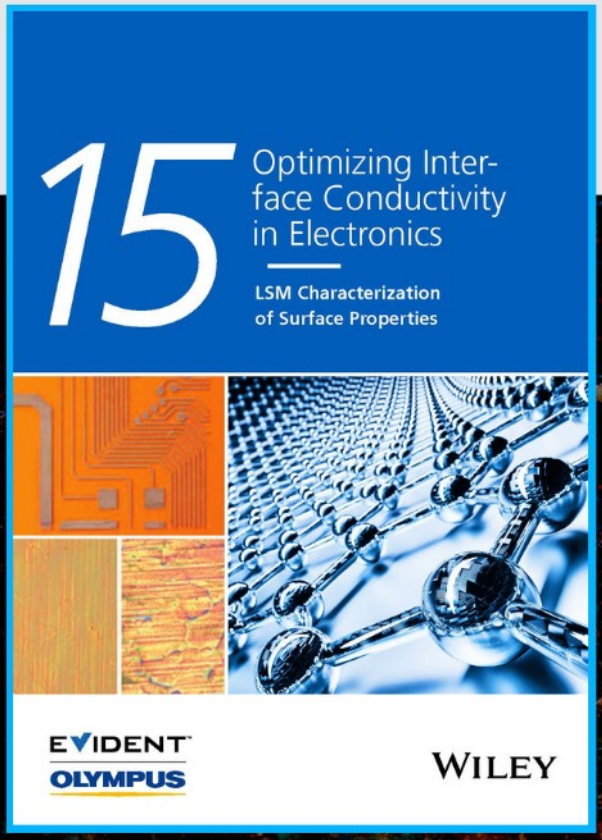

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Boolean Logic Computing Based on Neuromorphic Transistor

Yifei Wang, Qijun Sun, Jinran Yu, Nuo Xu, Yichen Wei, Jeong Ho Cho,* and Zhong Lin Wang**

General-purpose computers usually use logic gate computing units based on complementary metal oxide semiconductors (CMOS). Due to the separate memory and computing units in Von Neumann architecture, data transmission requires great energy and time consumption. Developing novel neuromorphic devices and comprehensively investigating their logical computing mode are crucial to achieve high-performance and low-power neuromorphic computation. Here, a systematic summary of Boolean logic computing based on emerging neuromorphic transistors is presented. This summary encompasses logical operation modes, materials, device structures, and working mechanisms. The input mode of Boolean logic operation is classified into electrical input, optical input, and synergistic optical/electrical input. Besides, additional modulation strategies to construct programmable logic functions by electrical, optical, and thermal signals are also summarized. These strategies hold great significance as they enable dynamic reconfiguration of logic operations and provide neuromorphic devices with decision-making capabilities. Finally, the application prospects and current challenges to Boolean logic computing based on dendritic integration are discussed from the aspects of device integration, synergistic input/modulation modes, auxiliary peripheral circuit, software/hardware system, etc. It is believed that comprehensive investigations on neuromorphic Boolean logic operations are crucial to push forward the development of future neuromorphic computing toward high efficiency and high integration density.

1. Introduction

Logic gates are the basic structure of digital systems to build general-purpose computers. However, general-purpose computers rely on the von Neumann architecture of separate memory and computing units, which necessitates frequent data transmission between the memory module and computing unit, leading to substantial energy consumption and time inefficiency.[1] In addition, the logic gate computing units based on complementary metal oxide semiconductors (CMOS) are limited by complex circuit design and high static power consumption.[2] In order to overcome the constraints imposed by the von Neumann architecture and separate data storage and logical computation, it becomes imperative to explore novel logical units and computing systems. One promising avenue to explore for solutions lies in the biological system, where the dendrites of a single neuron can receive and process multiple input signals from hundreds of surrounding neurons. Accordingly, the biological nervous system can be considered as an in-memory computing system (i.e., the memory and logic computing

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functions into a single entity), which can significantly improve the processing speed of data-intensive computation and reduce energy consumption.[1,3–5] Emerging novel neuromorphic device is the basic unit for high-performance logic computing, and its most important feature is the nonvolatile memory effect, which allows the neuromorphic device to store the data in-situ and perform logical operations simultaneously. The process of nonvolatile logic gate computing is similar to that of updating the dynamic weights in biological synapses, which enables high-performance memory computing beyond CMOS without static power consumption.[6] Therefore, developing novel neuromorphic devices and comprehensively investigating their logical computing mode are crucial to realize high-performance and low-power neuromorphic computation.

To date, neuromorphic transistors based on low-dimensional materials,[7–9] oxides,[10] inorganics,[11–13] and organics[14] have been extensively researched and reported. These materials are primarily utilized to emulate the biological synaptic behaviors achieved through electrolyte gating (EG),[15] phase change (PC),[16–17] ferroelectric (FE) domain switching,[18] or other mechanisms.[19–20] One notable feature of these neuromorphic transistors is their ability to receive multiple input signals and perform Boolean logic operations through dendritic integration. This characteristic allows them to avoid hardware redundancy and system delay issues typically encountered in conventional CMOS technology-based computing.[21–22] Notably, the sophisticated properties of logic operations in one single device and the interactive functions with multiple external stimuli in neuromorphic transistors are not available in another typical neuromorphic device based on memristors. Consequently, neuromorphic transistors possess a significant advantage in terms of logic functions.

In this review, we systematically investigate and summarize the Boolean logic operations based on neuromorphic transistors, including the logical operation modes, materials, device structures, and working mechanisms. First, a concise introduction is provided on conventional CMOS technology neuromorphic transistors for Boolean logic operations. Then we highlight emerging neuromorphic transistors capable of receiving multiple and synergistic input signals to perform sophisticated logic operations. The input mode of Boolean logic operation is classified into electrical input, optical input, and synergistic optical/electrical input. Electrical input is the most common activation method for neuromorphic transistors, which generally requires the construction of multiple gates for electrical inputs; optical input can simulate the way humans perceiving the external environment and has greater bandwidth and faster signal processing speed[23]; synergistic optical/electrical input is feasible to conduct multiple combined input modes and promises a high degree of flexibility on the updating of synaptic weight. In addition to multiple input modes, neuromorphic transistors are also able to switch among various Boolean logic gates through the modulation of input terminals by additional electrical or optical signals. The programmable logic functions can dynamically reconfigure logic operations and enable neuromorphic transistors to have certain decision-making capabilities. Current neuromorphic computing only demonstrates basic Boolean logic gate operations without combinatorial logic computation and functionalization, which limits its application prospects. Relevant prospects and possible strategies are proposed and discussed at the end of the review. We believe that building neuromorphic computing with high-performance computing efficiency and integration will be one of the mainstreams toward future computation.

2. The Principles of Boolean Logic Operations: Conventional CMOS Logic Circuits Versus Neuromorphic Dendritic Integration

Logic gates are commonly composed of resistors, capacitors, diodes, and transistors, which are the basic components of integrated circuits. The basic Boolean logic operation generally requires two input transistors, which use high and low electrical levels to represent the logical "True" and "False" (or "1" and "0" in binary). As commonly known, there are six basic logic gates: "AND", "OR", "XOR", "NAND", "NOR", and "NXOR". Their respective truth table is shown in **Figure 1**a. Taking the AND logic gate as an example, the output is high level only when all inputs are high level (logic "1"); otherwise, the output is low level (logic "0"). Based on the combination of basic logic gates, more complicated logic circuits and digital functions can be achieved. For instance, the half adder combines an AND and an XOR logic unit, in which the input is "Sum" after the XOR operation and "Carry" after AND operation; the adder is composed of one OR logic gate and two half adders to implement multibit addition; the combination of adders and AND logic gates can realize multiplication. Conventional logic circuit based on CMOS gates has low static power consumption, strong anti-interference ability, high switching speed, and reliable operation. A common Boolean logic gate requires 4 or 6 CMOS silicon transistors. As shown in Figure 1b, the logic gate circuit in orange color represents a CMOS-based AND, while the remaining black-colored circuit represents a NAND logic gate. Some reported half-adder circuits even require 16 transistors, including 5 transistors to form an AND logic gate, and 11 transistors to form an XOR logic gate.[24] Accordingly, it is critical to construct new logic devices to use fewer transistors and realize more compact integration.[25]

The emergence of novel neuromorphic devices provides a new way to solve such problems, aiming to imitate the function of a brain composed of a large number of neurons to form a highly complex neural network and information processing center (Figure 1c). A single biological neuron comprises of dendrites, axon, and soma (Figure 1d), which commonly has multiple dendrites to receive, integrate, and filter complex input information from pre-neuron (PREN). The dendrites serve as the primary input structures in a neuron, transmitting signals from the synapses with PRENs to the post-neuron (POSTN) via the axon terminal. The dendrites are capable of conducting information integration through both linear and nonlinear algorithms, a process known as dendritic integration.[26–28] In the context of dendritic integration, super-linear dendritic integration occurs when synchronous inputs from multiple synapses trigger an excitatory postsynaptic current (EPSC) that exceeds the sum of EPSC from individual synaptic inputs. This phenomenon is typically observed when the input signals are imposed from the same dendritic branch. Conversely, linear dendritic integration takes place when the EPSC triggered by synchronous inputs from multiple synapses is equal to the sum of individual EPSC. This

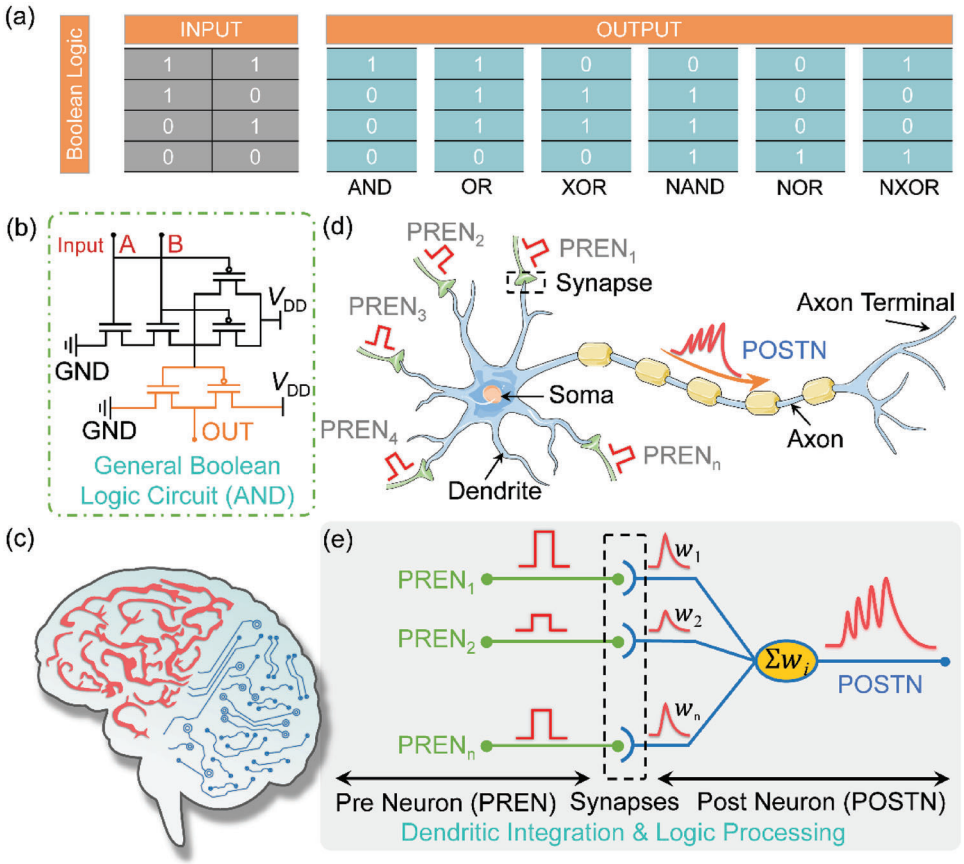

Figure 1. Boolean logic operations based on conventional logic circuits and dendritic integration. a) Truth table of basic Boolean logic gates. b) General Boolean logic circuit based on conventional CMOS logic circuits. c) Schematic diagram of the brain. d) Schematic diagram of the structure of a single biological neuron. A neuron is mainly composed of dendrites, axon, and soma. e) Simplified biological neuron system. It contains multiple input signals from pre-neurons (PREN) and one output signal from post-neuron (POSTN).

type of integration commonly occurs when the input signals are imposed from different dendritic branches. Lastly, sublinear dendritic integration arises when the EPSC triggered by synchronous input signals from multiple synapses is smaller than the sum of individual EPSC.[29] Understanding dendrite mechanisms are therefore critical for comprehending the information transmission between neurons and improving the overall performance and efficiency of dendritic integration in biological system.[30–31]

Figure 1e displays a simplified biological neuron system with multiple PREN input signals and one POSTN output signal, and this structure is a single-layer neural network. As the signals from PREN often have different intensities, the weights (w_i) of these input signals should be adjusted by matrix-vector multiplication and then integrated. If the integration signal (Σw_i) exceeds the threshold, the POSTN will trigger the execution of the action.[32] Inspired by the biological neuron system, neuromorphic transistors have the capacity to integrate and process multi-input information. This capability enables them to bestow conventional Boolean logic operations with a more sophisticated and advanced approach. For instance, the requirements of complex wiring and a large number of conventional CMOS transistors can be avoided by using the dendritic integration capability of a single neuromorphic transistor, which is of great significance to build artificial neural networks with high integration and computing efficiency in future.[33–34]

3. Boolean Logic Operations in Neuromorphic Transistors Based on CMOS Technology

The utilization of CMOS technology to construct logic gate circuits is a common approach to implementing Boolean logic operations in neuromorphic transistors. In CMOS-based logic devices, n-type and p-type transistors often appear in pairs. Taking 2D trending materials as an example, the dynamic regulation of 2D FET between p-type and n-type can be realized by imposing different electric fields. Chen et al. use bipolar WSe_2 as the channel material to prepare a double-gate transistor.[35] As shown in **Figure 2**a, by adjusting the polarity of the dual gates (V_{gA} and V_{gB}), the device can be tuned between n-n, n-p, p-p, and p-n types. For example, when the V_{gA} input is greater than 0 V and the V_{gB} input is less than 0 V, an n-p type device is obtained, i.e., a CMOS structured logic device. Furthermore, as the charge carrier flow direction in the device channel can be reversed by changing the polarity of drain voltage (V_{ds}), the authors successfully realize a reconfigurable logic function

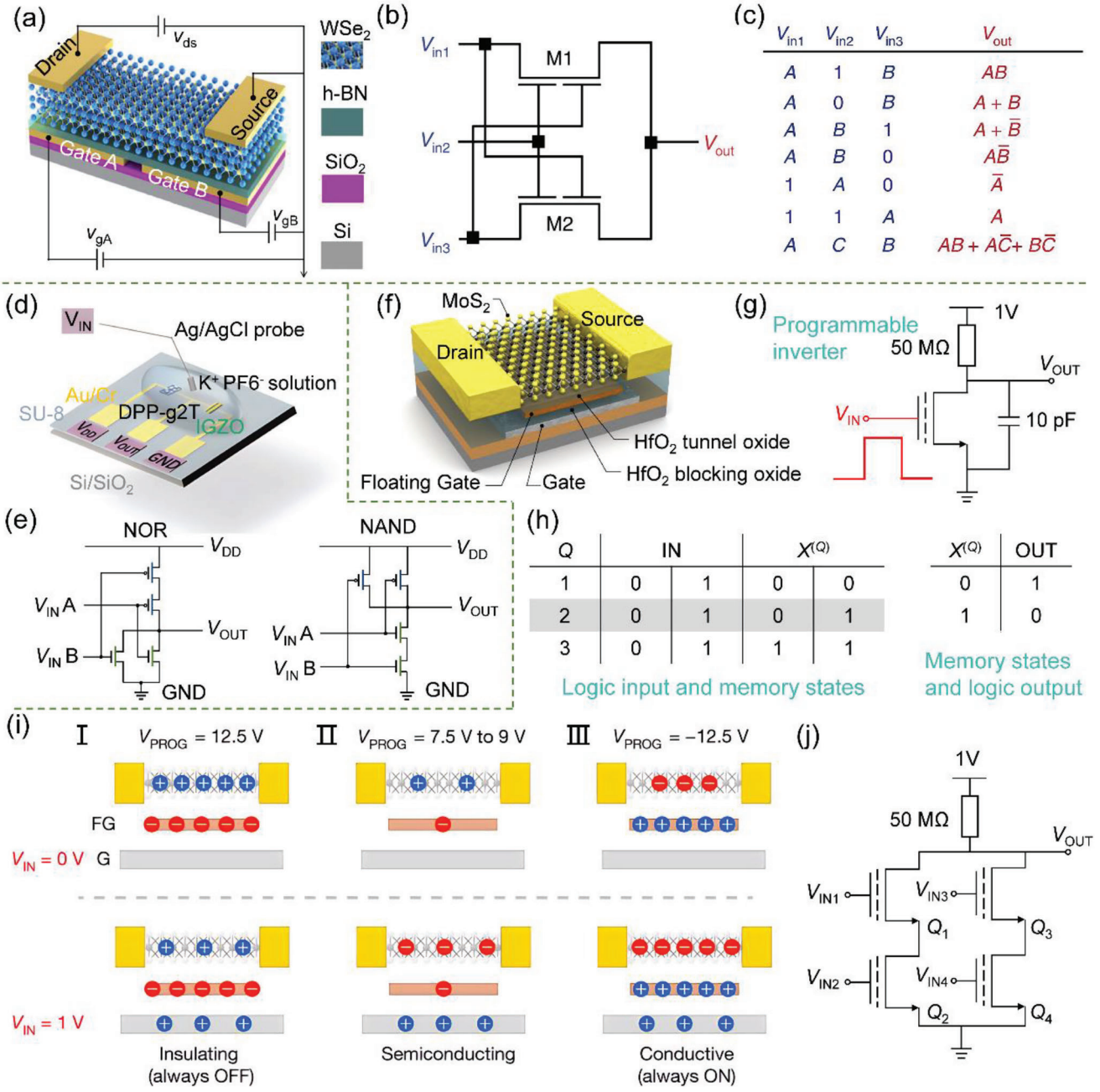

Figure 2. Boolean logic operations in neuromorphic transistors based on CMOS technology. a) Structural diagram of a dual-gate transistor based on a bipolar WSe_2 channel. Reproduced with permission.[35] Copyright 2020, Springer Nature. b,c) The reconfigurable logic function circuit constructed by two WSe_2 transistors and the corresponding logic operations. Reproduced with permission.[35] Copyright 2020, Springer Nature. d,e) Structural diagram of a CMOS device based on an electrolyte-gated transistor (EGT) and the corresponding Boolean logic operation circuit. f) Schematic diagram of the MoS_2-based floating-gate field-effect transistor (FGFET). Reproduced with permission.[43] Copyright 2020, Springer Nature. g) Circuit schematic of the programmable inverter. Reproduced with permission.[43] Copyright 2020, Springer Nature. h) The relationship table among FGFET's floating gate storage state (Q), logic input (IN), memory logic state ($X^{(Q)}$), and output voltage (OUT). Reproduced with permission.[43] Copyright 2020, Springer Nature. i) Schematic illustration of the three storage states of the floating gate. j) Dual-input logic memory unit. Reproduced with permission.[43] Copyright 2020, Springer Nature. Logic gate operations including NAND, NOR, XOR, etc. can be performed by adjusting the pre-storage state ($Q_{1\text{-}4}$) in the floating gate of each device. Reproduced with permission.[43] Copyright 2020, Springer Nature.

circuit by using two gate terminals (V_{gA} and V_{gB}) and the V_{ds} as input signals to cascade two devices (Figure 2b). Figure 2c indicates the statistical output results of the reconfigurable logic function circuit under different input states (logic "1" as the high voltage input, logic "0" as the low voltage input). By adjusting the input state of V_{IN2}, the logic conversion of AND gate (AB) and OR gate (A+B) can be achieved. In addition, this reconfigurable logic function circuit also realizes other logic gate functions, including material implication (IMP) gate (A+$\bar{B}$), not material implication (NIMP) gate (A$\bar{B}$), inverter ($\bar{A}$)), follower (A), and borrow output (Bout) (AB+A$\bar{C}$ +B$\bar{C}$). Notably, through the cascade of the three devices, the synaptic spike-timing-dependent plasticity (STDP) and plasticity enhancement/inhibition functions can also be imitated.[36–37]

In addition to 2D materials-based CMOS devices, electrolyte-gated transistor (EGT) is also intensively investigated for logic gates and recently emerging neuromorphic transistors due to its unique electric double layer (EDL) that can continuously regulate channel carriers.[38–41] Yao et al. report an EGT based on a p-type organic electrochemical transistor (OECT) and an n-type electric double-layer transistor (EDLT) (Figure 2d).[42] Based on the electrolyte-gated device, the authors fabricate NOR and NAND logic gates through the extended circuit as shown in Figure 2e. In addition to the CMOS cascading expansion, Marega et al. explore the utilization of a floating gate field effect transistor (FGFET) prepared by large-area MoS_2 to realize the function of programmable logic (device structure in Figure 2f).[43] FGFET, as the earliest reported neuromorphic transistor, can effectively implement programmable logic functions by changing the state of stored charges in its floating gate.[44] Figure 2g shows the circuit diagram of the programmable inverter, in which the gate is used to set the charge storage state of the floating gate and as the input terminal (V_{IN}) for logic operations. The V_{IN} inputs of 0 and 1 V correspond to logic outputs of "0" and "1", respectively. The resultant relationship of floating gate storage state (Q), logic input (IN), memory logic state ($X^{(Q)}$), and output voltage (OUT) is shown in Figure 2h. The three states of Q indicate the charge storage states in Figure 2i (I-III). For the states $Q = 1$ and $Q = 3$, due to the strong charge doping in the floating gate, the input cannot influence the output as the channel remains closed ($Q = 1$) or open ($Q = 3$). For the state of $Q = 2$, the weaker charge doping in the floating gate makes the device state directly reflect the input logic state ($X^{(2)}$ = IN), allowing the circuit to operate as an inverter. On this basis, the authors also propose a dual-input logic memory unit (Figure 2j). By adjusting the pre-stored state ($Q_{1\text{-}4}$) in the floating gate of each device, any logic operation including NAND, NOR, XOR, and other logic gates can be conducted. The development of reconfigurable logic based on emerging neuromorphic transistors are critical to high-performance computing in the future.

4. Boolean Logic Operations in Neuromorphic Transistors Based on Dendritic Integration

The neuromorphic transistors summarized above are based on CMOS technology to build n-p type structure or to implement inverter function for Boolean logic operations. In contrast, neuromorphic transistors also offer the capability of dendritic integration, enabling a single device to carry out multiple Boolean logic operations and logic conversions. Since 2016, significant advancements have been made in the field of Boolean logic operations based on neuromorphic transistors. In this review, we focus on the Boolean logic operations implemented by neuromorphic transistors (the development timeline is shown in **Figure 3**). The modulation strategy for performing Boolean logic operations is classified into electrical input,[45–49] optical input,[34,50] and synergistic optical/electrical input,[29,51–52] and recently emerging triboelectric[47] and thermal[49] modulation. By utilizing diverse signal input and modulation strategies, reported devices show different Boolean logic operation capabilities. Some devices demonstrate a single Boolean logic operation, while others exhibit the capability to achieve logic gate conversion or reconfigurable logic through the modulation (i.e., a single device can realize the conversion of AND and OR logic gates). Additionally, the utilization of diversified modulation signals is crucial for neuromorphic transistors to accurately simulate real environmental perception. Moreover, incorporating multiple/hybrid modulation modes can further expand the functionalization of neuromorphic transistors. During the discussion of different modulation strategies, the classification of active materials and device structures is further refined within each modulation type. It is believed that neuromorphic transistors will endow the Boolean logic operations with more sophisticated characteristics, providing new solutions for the next generation of interactive in-memory computing and multi-modal, low-power, and large-scale intelligent systems with neuromorphic features.[53]

5. Boolean Logic Operations Based on Electrical Input: Electronic Boolean Logic

Electrical input serves as the primary and most crucial method of input for neuromorphic transistors, facilitating effective regulation of channel carriers through the application of electrical stimulation to the gate. Typically, implementation of multiple spatiotemporal inputs requires the fabrication of multiple gates.

5.1. Electrical Input-Based Boolean Logic Operations

Figure 4a shows the schematic illustration of the neuron structure by electrical modulation. In this section, we introduce the Boolean logic operation solely based on electrical input. Devices that fall into this category can realize AND, OR, or other logic gate operations through dendrites integrating two electrical inputs. Neuromorphic transistors based on one-dimensional (1D) nanomaterials usually use polymer electrolytes as gate dielectrics. When a low voltage is applied, the ions present in the polymer electrolyte migrate directionally, creating an EDL at the interface between the active semiconducting layer and the gate-insulating layer. This formation of the EDL induces EPSC within the nanowire channel.[54–56] Usually, the gate electrode acts as the pre-synapse, and the nanowire channel corresponds to the post-synapse. In addition, combining 1D nanomaterials with polymer electrolytes has many excellent physicochemical properties[57–58]; Due to the high specific surface area, 1D nanomaterials (e.g., nanowires, nanorods, nanofibers) can provide better conductive channels for ions at the interface between the active materials and

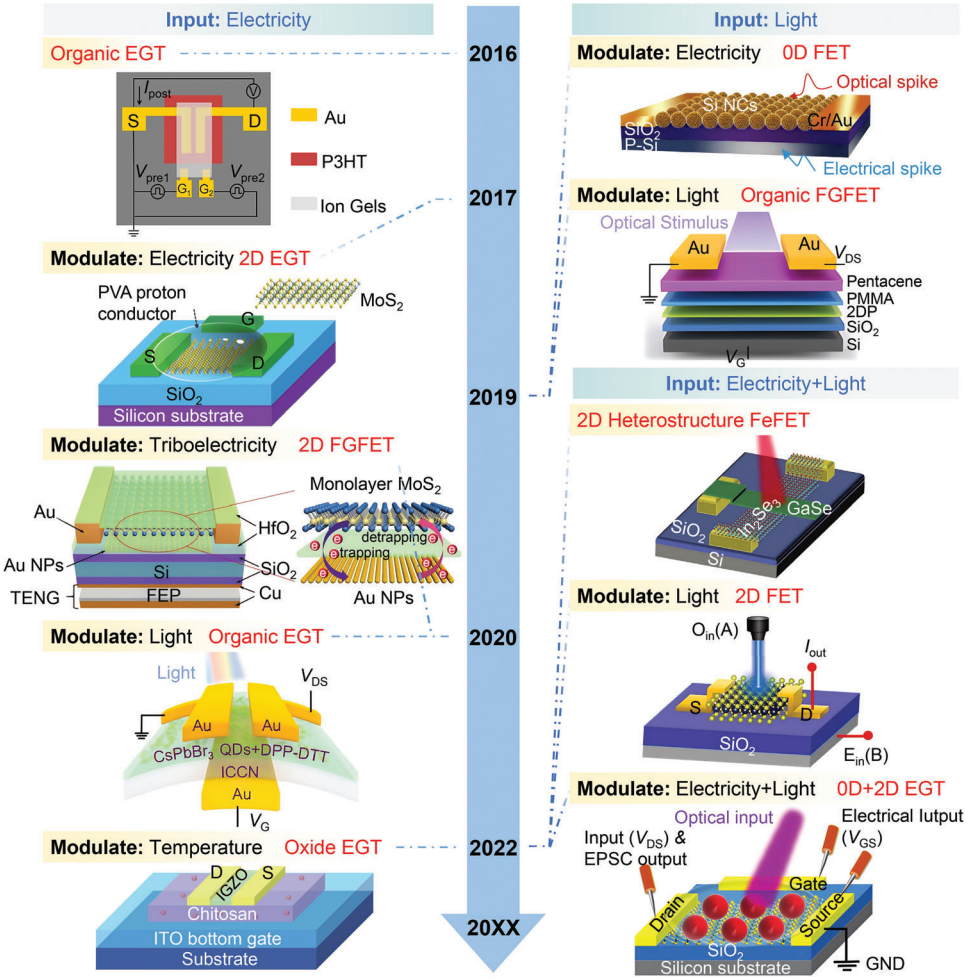

Figure 3. Development timeline of Boolean logic operations in neuromorphic transistor based on dendritic integration.

the electrolyte so as to enhance the ionic conductivity. In addition, owning to the reduced Young's modulus of the 1D nanomaterials, the device can maintain high ionic conductivity even under a bending state.[59] Moreover, EGT is feasible for multigate structure combined with dendrite-like integration function to process multiple input signals simultaneously, allowing low-power consumption and sophisticated characteristics.[60] So far, many studies have demonstrated various organic electrolytes (e.g., chitosan, starch, and composite organic compounds) for the gate dielectrics of EGTs.[61] Zou et al. uses lithium perchlorate mixed with polyethylene oxide polymers ($PEO/LiClO_4$) as the electrolyte gate and SnO_2 nanowires as neuromorphic transistor channels (Figure 4b).[62] Lei et al. use polyvinyl alcohol (PVA) polymer as the gate dielectrics and $Li_7La_3Zr_2O_{12}$ (LLZO) nanofibers as the neuromorphic transistor channel (Figure 4c).[63] To realize the Boolean logic applications based on the neuromorphic transistors, they all adopt a dual-gate structure design to implement the input logic of "00", "01", "10", "11", corresponding to no voltage applied to G_1 and G_2, voltage applied to G_1, voltage applied to G_2, and voltage applied to G_1 and G_2 at the same time, respectively. The achieved output results of the AND logic gate are shown in Figure 4d. When the EPSC amplitude is greater than the threshold of 0.40 mA, it represents a logic "1", otherwise it represents a logic "0".

2D materials have exhibited significant potentials in information sensing, storage, and processing because of their unique layered structure, atomic thickness, large on/off current ratio, and high charge carrier mobility.[24,64–66] Based on the dynamic characteristics of biological synapses, 2D material transistors are widely adopted to emulate the function of biological synapses.[67–70] When it is combined with the unique structure of the FGFET, the 2D transistor is able to perform digital logic processing and data storage more effectively based on the nonvolatile logic operation characteristics and machine learning-assisted data analysis capacity. A 2D WSe_2 FGFET prepared by Hou et al. is demonstrated as a logic storage transistor with sensing-storage-processing functions.[71] According to the device structure in Figure 4e, the WSe_2 floating gate can be adjusted by both the bottom and top gates. When the logical input is "10" (positive bias on V_{BG} and negative bias on V_{TG}), the output current is $\approx 10^{-11}$ A to represent the logical output of "0" (Figure 4f). When the logical input is "11" (positive bias on both V_{BG} and V_{TG}), the output is $\approx 10^{-7}$ A, representing the logical output of "1" (Figure 4g). Furthermore, as the logic outputs can be stored

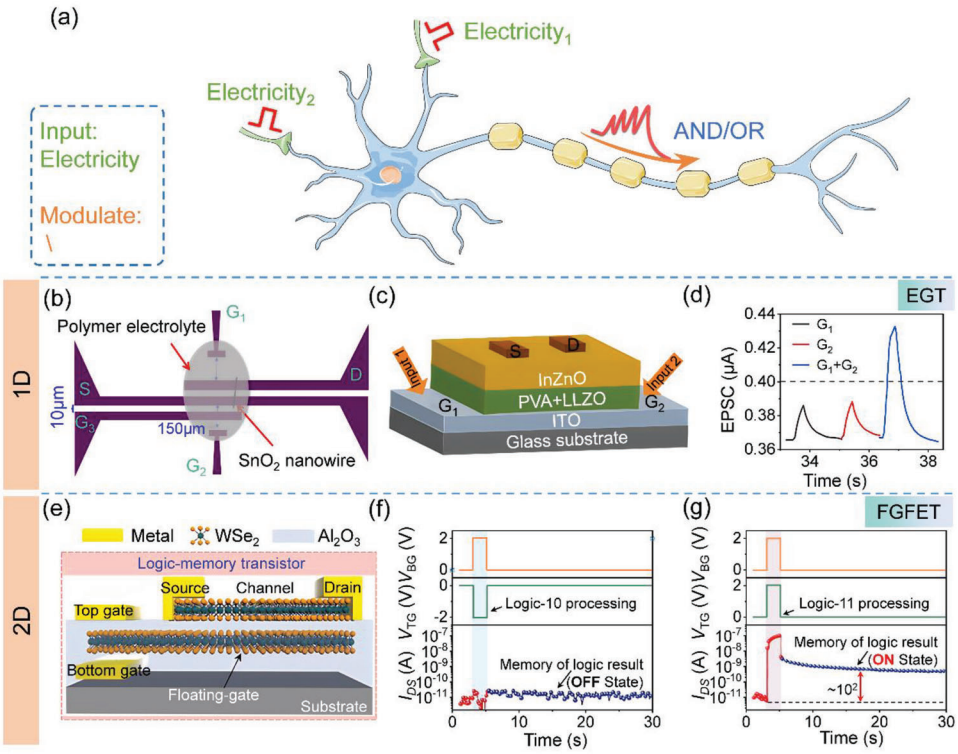

Figure 4. Electrical input-based Boolean logic operations of low-dimensional materials. a) Schematic diagram of neuron structure with dendrites integrating electrical input. Reproduced with permission.[62] Copyright 2017, Springer Nature. b) Structure diagram of EGT based on one-dimensional SnO_2 nanowires. c,d) Structure diagram of EGT based on $Li_7La_3Zr_2O_{12}$ (LLZO) nanofibers and the output results of AND logic gates. e) Structure diagram of FGFET based on WSe_2. f,g) The logical input and output results of WSe_2-based FGFET when the logic inputs are "10" and "11". This is AND logic gate.

in-situ in the device channel, the AND logic gate can be implemented through a single FGFET without additional storage units and operations. Therefore, the device can be highly integrated and functionalized.

The fourth-generation oxide semiconductor material represented by IGZO is a new generation of high-performance channel material, which has higher electron mobility, lower processing temperature, and better compatibility than amorphous silicon (α-Si).[72–73] For instance, Shao et al. demonstrate an IGZO EGT with sol-gel treated silicon dioxide electrolyte film as the gate dielectrics (**Figure 5**a).[74] The device is capable of working at a low voltage (<2 V) and achieves a high on/off ratio (>10^7). Kim et al. choose to use natural milk polymer as the gate dielectrics to prepare EGT with IGZO channels (Figure 5b).[75] The composition of cow's milk contains casein, lactose, and a large number of mobile protons.[76–77] It is the presence of protons in cow's milk that allows the device to exhibit typical EPSC behaviors through a strong capacitive coupling effect. Other natural protein materials have also been used for neuromorphic transistors, such as egg white protein, silk fibroin, and keratin, etc.[78–79] In terms of Boolean logic operations, this type of oxide-based neuromorphic transistor also uses two coplanar gates as two presynapses for logic inputs. As shown in Figure 5c, the output result takes EPSC 300 nA as the threshold, and the amplitude is greater than 300 nA as the logic result "1", otherwise it is "0". Based on the super-linear spatial summation behavior of neuromorphic transistors, the AND logic operation is successfully implemented.

Organic semiconductor transistors are also promising for neuromorphic transistor applications due to good flexibility, biocompatibility, low cost, and excellent process compatibility.[80–81] Qian et al. employ poly(3-hexylthiophene) (P3HT) as the channel and ion gel as gate dielectrics to prepare organic EGT for biological synaptic behaviors (Figure 5d). In this organic artificial synapse, the presence of mobile ions $[TFSA]^-$ in the ion gel dielectrics plays a decisive role in triggering the EPSC—the open structure of P3HT enables the doping of ions when subjected to an electric field. In terms of Boolean logic applications, as shown in the structure diagram, two coplanar gates are used as input terminals. The logical input and output results are shown in Figure 5e. The EPSC amplitudes induced by two individual gate voltages are −1.2 and −1.26 μA, respectively, which are slightly smaller than the cotriggered EPSC amplitude of −1.53 μA. Based on the sublinear dendritic integration behavior of neuromorphic transistors, the OR logic gate operation is successfully realized.

An inorganic EGT is proposed by Wei et al. with SnO_2 nanoparticles (SONPs) as channel materials and electrolyte/polymethyl methacrylate (PMMA) films on poly (ethylene naphthalate) flexible substrates as gate dielectrics (Figure 5f).[82] Electrolyte/PMMA membrane is used to simulate the synaptic cleft. The migration behavior of Li^+ in the electrolyte is similar to that of synaptic neurotransmitters, which is used to induce EPSC.[67] In addition, under the action of an electric field, Li^+ ions will be electrochemically doped into the SONP channel. PMMA as a modified layer can reduce the electron traps at the

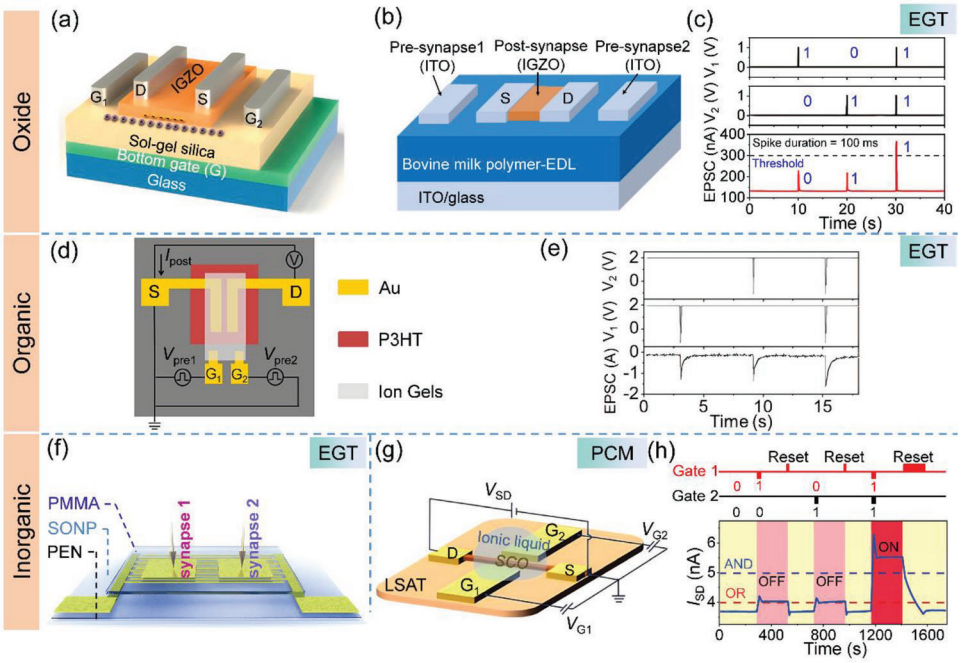

Figure 5. Electrical input-based Boolean logic operations of bulk materials. a) Structure diagram of EGT based on IGZO and sol-gel treated silica electrolyte. b,c) Structure diagram of EGT based on IGZO and milk polymer electrolyte, and the input and output results of the corresponding AND logic gate. d,e) Structure diagram of organic EGT based on poly(3-hexylthiophene) (P3HT) and ion gel electrolyte, and the input and output results of the corresponding OR logic gate. f) Structure diagram of EGT based on SnO_2 nanoparticles (SONPs) and electrolyte/PMMA film as gate dielectric. Reproduced with permission.[82] Copyright 2021, Elsevier. g,h) Structure diagram of neuromorphic transistor based on inorganic phase change material (PCM) $SrCoO_x$, and the corresponding Boolean logic input and output results. The AND and OR logic gates are only switched by different threshold settings. Reproduced with permission.[17] Copyright 2019, John Wiley and Sons.

electrolyte/channel interface and alleviate the volume expansion of device channel caused by electrochemical doping.[83–84] In the application of Boolean logic, the inorganic neuromorphic transistor uses two coplanar gates to construct multiterminal input to simulate the logic operation ability of parallel information processing.[85] In addition, the influence of different input intervals on the results of AND logic gates is studied, which is highly fault-tolerant under high-frequency operations. Huang et al. propose a neuromorphic transistor based on an inorganic phase change material (PCM) with $SrCoO_x$ (SCO) film as the channel (Figure 5g).[17] By applying gate bias, the channel materials can be doped by regulating the oxygen ions produced by the hydrolysis reaction of trace water in ionic liquid electrolytes. SCO can be reversibly transformed into limonite $SrCoO_{2.5}$ and perovskite $SrCoO_{3-\delta}$.[15,86] Thus, the channel can undergo a reversible transition between the low and high conductance states. When a negative gate voltage is applied, oxygen ions in the electrolyte are inserted into the channel material, causing the channel to transform into a high-conductance phase. Conversely, applying a positive gate voltage induces the extraction of oxygen ions from the channel, converting the channel into a low-conductance phase. Here, the gate electrode and the inorganic channel are used to simulate the presynapse and postsynapse of the biological neuron, respectively, and the oxygen ions in the electrolyte act as neuronal transmitters. In the application of Boolean logic operations, two coplanar gates are used as the logic input terminals (input 0 V defined as logic input "0", input −1 V defined as logic input "1"). The Boolean logic operation and logic output are shown in Figure 5h. By defining different EPSC threshold values (5 or 4 nA), the logic gates can be tuned between AND and OR function. The realization of multiple logic gates and nonvolatile logic output results are of utmost important for versatile neuromorphic computing.[87–88]

5.2. Electrical Modulation for Electronic Boolean Logic

Neuromorphic transistors with multiple presynaptic inputs can be modulated by multiple electrical signals or different types of electrical stimuli (e.g., triboelectricity, piezoelectricity, and pyroelectricity) to achieve dynamic modulation logic functions (**Figure 6**a). The neuromorphic transistors can realize various logic gate operations of AND, OR, NAND, and NOR by integrating two electrical inputs and a modulation signal through dendrites. Furthermore, the incorporation of nonvolatile memory properties into these logic gates enhances their effectiveness in machine learning and data analysis applications.[88–90]

2D materials can be effectively combined with various electrolytes to form EGTs, which offer a facile method for preparing multigate structures and performing various logic operations. Du et al. use 2H-MoS_2 as the semiconductor channel, and N,N-diethyl-N-(2-methoxyethyl)N-methylammonium bis(trifluoroform sulfonyl)imide ionic liquid as the gate dielectrics to prepare EGT (Figure 6b).[91] In EGTs, the top gate (Gate 1) and bottom gate (Gate 2) serve as two inputs, while the drain current is regarded as the output. When different electric

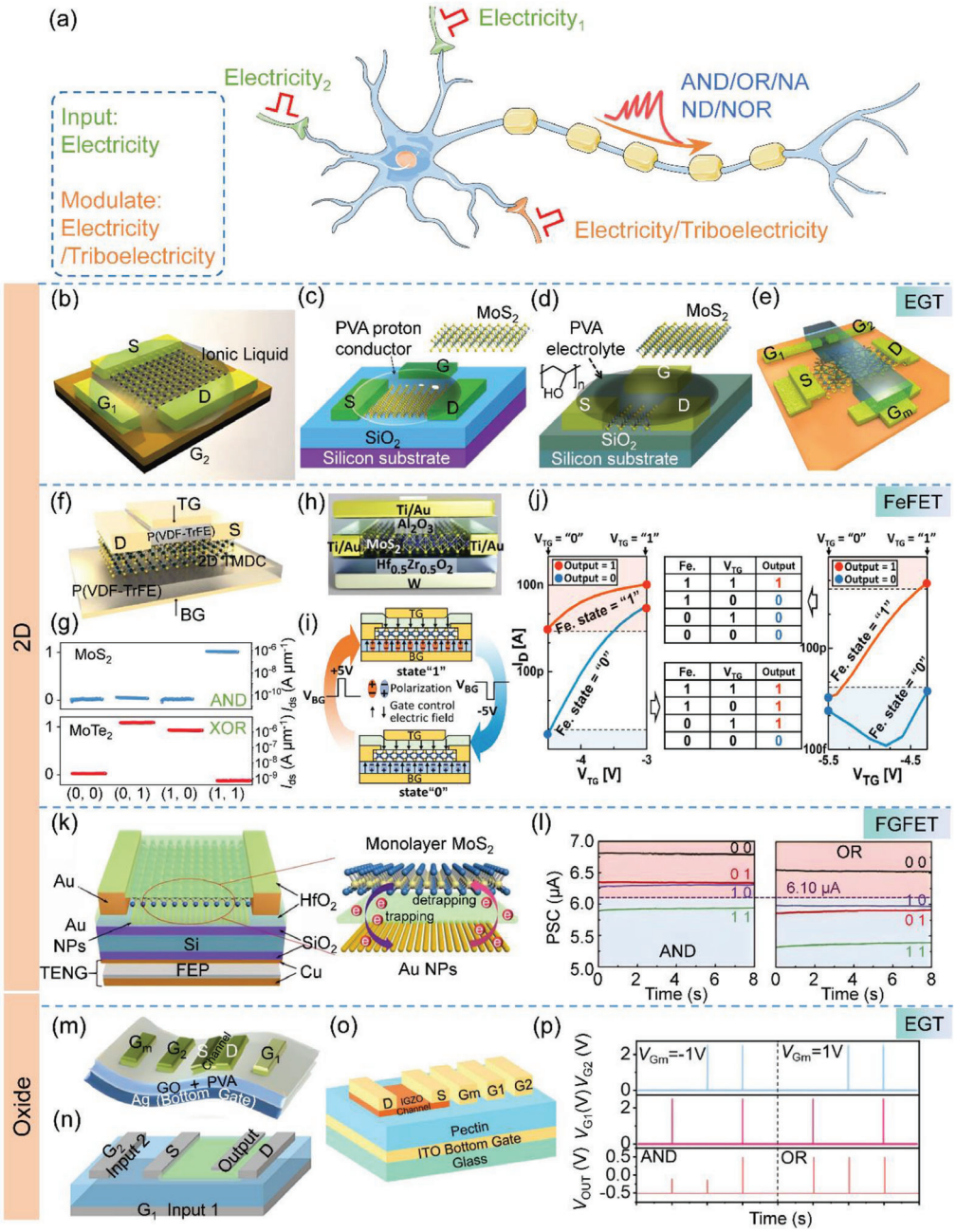

Figure 6. Boolean logic operations based on electrical input and electrical/triboelectric modulation. a) Schematic diagram of neuron structure with dendrites integrating electrical input and electrical/triboelectric modulation. b) Structure diagram of EGT based on MoS_2 and ionic liquid electrolyte. Reproduced with permission.[15] Copyright 2018, John WIley and Sons. c,d) Structure diagram of EGT based on MoS_2 and PVA electrolyte. Reproduced with permission.[19] Copyright 2018, Elsevier. Reproduced with permission.[46] Copyright 2017, John WIley and Sons. e) Structure diagram of EGT based on Graphdiyne (GDY)/MoS_2. Reproduced with permission.[93] Copyright 2021, John WIley and Sons. f) Structure diagram of 2D ferroelectric transistors (FeFET) based on unipolar MoS_2 and bipolar $MoTe_2$ as channel materials and P(VDF-TrFE) as ferroelectric gate dielectrics. g) The output result of AND gate operation performed by MoS_2-FeFET and XOR gate operation performed by $MoTe_2$-FeFET. h) Structure diagram of 2D FeFET based on MoS_2 as channel material and $Hf_{0.5}Zr_{0.5}O_2$ (HZO) ferroelectric as gate dielectric. i) The polarization field and logic state of ferroelectrics are adjusted by back gate bias (V_{BG}). V_{BG} = +5 V, HZO is a nonvolatile logical state "1". V_{BG} = −5 V, HZO is a nonvolatile logical state "0". j) Boolean logic input and output results based on HZO logic state and top gate input. AND and OR logic gates can be implemented. k) Structure diagram of FGFET based on MoS_2 as the channel material and Au nanoparticles (Au NPs) as the floating gate. l) The output of electrical signal is used as the logic input, and triboelectric nanogenerator (TENG) is used as the modulation terminal to perform AND and OR logic switching functions. Reproduced with permission.[98] Copyright 2020, Wiley. m) Structure diagram of EGT based on IGZO and graphene oxide (GO)/PVA electrolyte. n) Structure diagram of EGT based on IGZO and PVA electrolytes. Reproduced with permission.[99] Copyright 2021, Springer Nature. o,p) Structure diagram of EGT based on IGZO and pectin electrolyte, and the input and output results of corresponding AND and OR logic gate operations.

pulses are applied to the Gate 1 to change the conductance state of the transistor, the device can enable the conversion between AND and OR logic gates and exhibit a programmable logic operation function. Jiang et al. and Xie et al. use MoS_2 as the semiconductor channel and PVA as the electrolyte for proton transport to prepare 2D EGT (Figure 6c,d).[46,92] Yao et al. use Graphdiyne (GDY)/MoS_2 to prepare EGT (Figure 6e).[93] In these three studies, a three-terminal input structure is adopted, two of which are used as logic input gate terminals, and the other is used as logic modulation gate terminal (G_m). By changing the amplitude of the modulation terminal bias, the transistor conductance state can be adjusted, thereby realizing the conversion of AND and OR logic gates.

Ferroelectric materials have tunable and nonvolatile polarization characteristics, fast response, and long-term data retention capacity, so they are widely used in the construction of artificial neuromorphic transistors and have great advantages in nonvolatile logic gates and in-memory computing.[94–96] Luo et al. use stacked unipolar MoS_2 and bipolar $MoTe_2$ as channel materials, and use P(VDF-TrFE) as the top and back ferroelectric gate dielectrics to prepare 2D ferroelectric gate field-effect transistor (FeFET) and realize the non-volatile logic gate function (Figure 6f).[97] The top and back ferroelectric gates are used as two logic inputs. MoS_2-FeFET can perform AND logic gate operation, while $MoTe_2$-FeFET is used to perform XOR logic gate operation. The logic output results of the two devices are shown in Figure 6g. The AND and XOR logic gates can be combined to complete the operation of half adder. Huang et al. use MoS_2 channel paired with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) ferroelectric dielectrics (high coercive electric field and high dielectric constant) to prepare 2D FeFET (Figure 6h).[98] As shown in Figure 6i, by applying a +5 V pulse to the back gate, the HZO can be polarized to attract electrons in the channel, resulting in a nonvolatile state "1". Conversely, when a -5 V pulse is applied to the bottom gate, the HZO polarization will repel the electrons in the channel and become a nonvolatile state "0". Moreover, the top gate can be used as an additional input terminal. When the input value is set to −3 V (logic input "1") and −4.5 V (logic input "0"), the device can implement AND logic gate. When the input of the top gate is set to 5.5 V (logic input "0") and −4.3 V (logic input "1"), the device can implement OR logic gate with corresponding results in Figure 6j. Accordingly, the polarization state of HZO is preset by the back gate, and the logic conversion function can be realized by changing the top-gate input.

Yang et al. prepare a MoS_2 artificial synapse with multifunctional mechano-synaptic-plasticity by using Au nanoparticles (AuNPs) as the floating gate layer (Figure 6k).[47] Triboelectric nanogenerator (TENG), which can be readily used as a gate control, endows neuromorphic devices with multifunctionality and active cognition. A simple artificial neural network is demonstrated through three FGFETs to implement the logic conversion function of neural morphology between AND and OR. Three FGFETs are connected in parallel, in which two of them use electrical input as logic input, and the third device uses the triboelectric potential to implement the logic modulation process. The voltage input of 100 V and −100 V are regarded as logic input "1" and "0", and the logical output is shown in Figure 6l. When the EPSC threshold is set as 6.1 μA, the device can realize AND logic gate (or OR logic gate) with the triboelectric modulation voltage at −100 V (or 100 V). Therefore, the neuromorphic logic calculation can be mechanically switched through the triboelectric potential of TENG.

For oxide neuromorphic transistors, researchers commonly use IGZO as channel material and different electrolytes as gate dielectrics to effectively combine multigate to realize the function of programmable logic gate. For instance, Wang et al. employ graphene oxide (GO)/PVA composite solid electrolyte gate (Figure 6m).[28] Dai et al. use PVA as the dielectric layer (Figure 6n).[99] And Guo et al. explore the use of pectin as the electrolyte dielectrics (Figure 6o).[31] As shown in Figure 6p, when two of the three gates are used as logic inputs and changing the third input bias of the modulation terminal, the neuromorphic transistor can effectively realize the conversion between AND and OR logic gates.

5.3. Optical Modulation for Electronic Boolean Logic

In addition to electrical modulation, dendrites can also integrate optical and thermal stimulation as the modulation signals, and implement various logic gate operations of AND, OR, NAND, and NOR (**Figure 7**a). In the 2D materials family, the transition metal dichalcogenides (TMDCs), represented by MoS_2 and WS_2, have broad applications in the fields of photodetectors and memory devices due to their excellent optical characteristics.[100–102] Specifically, TDMC exhibits persistent photoconductivity (PPC), wherein it can trap photogenerated carriers through impurities and defects. As a result, even after the light source is removed, TDMC can sustain a photocurrent for a specific duration. This unique characteristic of PPC of TDMC allows its utilization in the development of diverse types of neuromorphic devices that simulate synaptic functions.[103–104] For instance, Zhang et al. construct a heterostructure phototransistor using WS_2/MoS_2 as shown in Figure 7b.[105] It adopts a dual-gate structure and uses graphene to lower the contact resistance. The dual-gate enables simultaneous modulation on the heterojunction at the WS_2/MoS_2 interface and the homojunction in WS_2, which is beneficial to enhance the performance of phototransistors. In terms of Boolean logic applications, the two gates are used as the input terminals of the logic (gate bias at 0 V is the logic input "1"; gate bias in negative value is the logic input "0"). In addition, the 532 nm light is used as the optical modulation signal (turning on the light is logic "1"; turning off the light is logic "0"). Corresponding logic input and output results are shown in Figure 7c. By setting the threshold at $\approx 10^{-9}$ A, and using the logic inputs "00, 01, 10, 11"along with a light modulation logic of "0", the resulting output is "0, 0, 0, 1". This configuration effectively implements an AND logic gate. Also, when the optical modulation logic is set to "1", the output result yields "1", thereby realizing an OR logic gate. In addition, when the voltages of −3 V and 0 V are applied to the back gate and the top gate, respectively, the homojunction formed at the interface between WS_2 and the gate electrode results in electron traps, and the trapping of photogenerated charge carriers due to the PPC effect. Therefore, after turning off the light, the drain current in Figure 7c (marked in the circle) shows a gradual and slow decrement. This outcome holds significant advantages for emulating the migration process of neurotransmitters in biological synapses.[106–108]

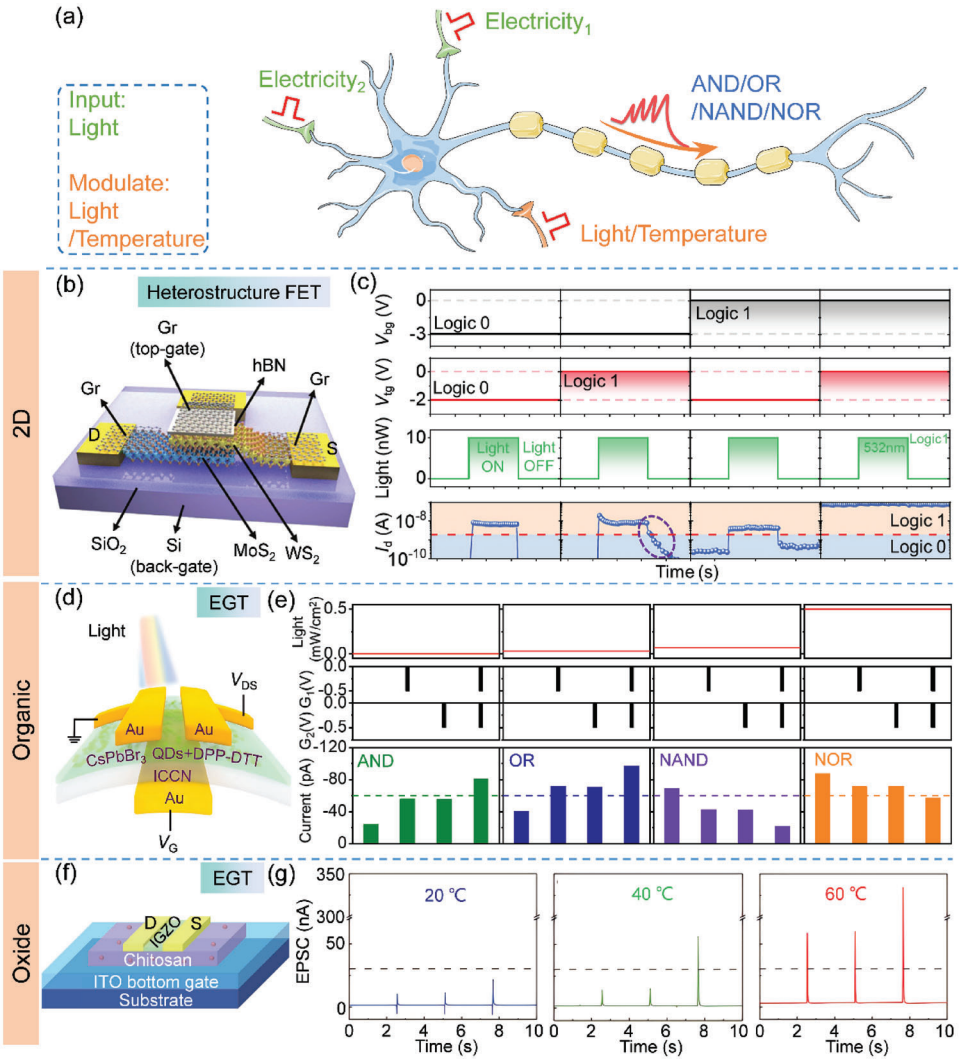

Figure 7. Boolean logic operations based on electrical input and optical/thermal modulation. a) Schematic diagram of neuron structure with dendrites integrating electrical input and optical/thermal modulation. b,c) Schematic diagram of WS_2/MoS_2 heterostructure transistor and the corresponding input and output results of Boolean logic performed based on electrical input and optical modulation. This operation implements the coupling of AND and OR logic gates. d,e) Schematic diagram of the EGT based on $CsPbBr_3$ combined with organic semiconductor DPP-DTT as channel material and ion-conducting cellulose nanopaper (ICCN) as electrolyte, and corresponding input and output results of Boolean logic performed based on electrical input and optical modulation. Reproduced with permission.[48] Copyright 2022, Elsevier. This operation realizes the conversion of the four logic gates of AND, OR, NAND, and NOR. f,g) Schematic diagram of the structure of the EGT based on IGZO and chitosan electrolyte, and the output results of implementing Boolean logic based on electrical input and temperature modulation. Reproduced with permission.[49] Copyright 2022, Springer Nature. This operation implements the conversion from AND to OR logic gates as the temperature increases.

Inorganic perovskite $CsPbBr_3$ quantum dots (QDs) have been widely used in the field of optoelectronics thanks to their excellent light absorption and narrow exciton binding energy.[109–111] Zhang et al. use $CsPbBr_3$ in conjunction with organic semiconductor DPP-DTT as the channel material, while utilizing ionically conductive cellulose nano-paper (ICCN) as the gate dielectrics to prepare an optoelectronic EGT (Figure 7d).[48] $CsPbBr_3$/DPP-DTT exhibits light-responsive behavior, while ICCN can form an EDL when subjected to electrical modulation. This unique combination allows the phototransistor to emulate synaptic characteristics and operate efficiently at ultralow voltages. In terms of Boolean logic applications, two coplanar gates are used as logic inputs, and the light is used as the modulation strategy to trigger the conversion of different logic functions. The device represents a logic "0" input under no gate bias condition. When a negative pulse is applied (representing a logic "1") without optical modulation, the device functions as an AND logic gate. In the presence of weak light modulation, the device can function as an OR logic gate. Conversely, if a positive pulse is applied (also representing a logic "0"), the device can operate as a NOR logic gate under weak light modulation. However, under strong light modulation, the device functions as a NAND logic gate, exhibiting the opposite behavior. Corresponding logic input and output results are shown in Figure 7e (setting the threshold at −60 pA). The above work demonstrates that one single neuromorphic transistor can realize the conversion of various Boolean

Table 1. Boolean logic operations based on electrical input.

Modulation strategy	Type	Device structure	Channel materials	Gate dielectric	Logic	Ref.
\	1D	EGT	SnO_2 NW	$PEO/LiClO_4$	AND	[62]
		EGT	InZnO	PVA/LLZO	AND	[63]
	2D	FGFET	WSe_2	Al_2O_3	AND	[71]
	Oxide	EGT	IGZO	Sol-gel Silica	AND	[74]
		EGT	IGZO	Bovine milk polymer	AND	[75]
	Organics	EGT	P3HT	Ion Gels	OR	[45]
	Inorganic	EGT	SnO_2 NP	Li^+ electrolyte	AND	[82]
		PCM	$SrCoO_{2.5}$	Ionic Liquid	AND, OR	[17]
Electricity	2D	EGT	MoS_2	Ionic Liquid	AND/OR	[91]
		EGT	MoS_2	PVA Proton Conductor	AND/OR	[46]
		EGT	MoS_2	PVA Electrolyte	OR	[92]
		EGT	GDY/MoS_2	Li^+ electrolyte	AND/OR	[93]
		FeFET	MoS_2, $MoTe_2$	P(VDF-TrFE)	AND/OR, XNOR/OR	[97]
		FeFET	MoS_2	$Hf_{0.5}Zr_{0.5}O_2$, Al_2O_3	AND/OR	[98]
Triboelectricity		FGFET	MoS_2	HfO_2	AND/OR	[47]
Electricity	Oxide	EGT	IGZO	PVA/GO	AND/OR	[28]
		EGT	IGZO	\	AND/OR	[99]
		EGT	IGZO	Pectin	AND/OR	[31]
Light	2D	Heterostructure FET	WS_2/MoS_2	HfO_2	AND, OR	[105]
	Organic	EGT	$CsPbBr_3$+DPP-DTT	ICCN	AND/OR/NAND/NOR	[48]
Temperature	Oxide	EGT	IGZO	Chitosan	AND/OR	[49]

logic gates by comodulation of electricity and light, which greatly enriches the synaptic plasticity of the device for information processing.

5.4. Thermal Modulation for Electronic Boolean Logic

Organic semiconductors exhibit sensitivity to ambient temperature, making them highly suitable for implementation in transistors. In thermal-sensitive neuromorphic transistors, temperature-sensitive electrolytes can be utilized as gate dielectrics to effectively regulate synaptic plasticity. This regulation is achieved through the influence of thermodynamic processes within the electrolyte, which directly impacts the migration of ions or protons involved in synaptic function.[112–113] Zhu et al. fabricate temperature-sensitive IGZO neuromorphic transistors with chitosan electrolyte gate dielectrics (Figure 7f).[49] Two coplanar gates are used for logic gate input, and the EPSC threshold of the logical output result is set at 30 nA. The logical output results at different temperatures are shown in Figure 7g. At 20 °C, all the logical operation results are less than the threshold. At 40 °C, the logic input is "11", and the EPSC is about 56.1 nA, which corresponds the logic result "1" (this is the AND logic gate). When the temperature reaches 60 °C, at the logic input of "10" and "01", the EPSC is ≈58.6 and 60.0 nA, corresponding to the logical result of "1" (this is the OR logic gate). The logic conversion by changing external temperature provides a new way for Boolean logic operation, playing a crucial role in the realization of a bionic perceptual neuromorphic system.

5.5. Section Summary

In **Table 1**, we summarize different Boolean logic operations based on electrical inputs. In both low-dimensional materials and bulk materials, a wide range of electrolytes are predominantly used as gate dielectrics. The electrolyte dielectrics can effectively regulate the conductance state of the channel for simulating synaptic function due to long-range polarization in electrolyte dielectrics. This allows construction of coplanar multigate structures and their ease of use in Boolean logic operations. The function of a single logic gate, e.g., an AND logic gate, can be realized by adopting two-gate architecture. Moreover, adding a third gate and changing its bias voltage allows advanced logic operation switching the logic gates to realize a programmable logic, e.g., AND and OR logic gates. This multigate structure can imitate the integration function of dendrites to process multiple input signals simultaneously. Furthermore, the electrolyte-gated neuromorphic transistors can be constructed by using photoresponsive materials as channels, which implements the logic

conversion by adjusting the optical power without the third gate. In addition, the utilization of temperature-sensitive electrolytes including chitosan enables perfoming the logical conversion of AND and OR logic gates by manipulating temperature. This advancement holds implication for the development of bionic-sensing neuromorphic systems. In addition to EGT, FeFETs with ferroelectric gate dielectrics and FGFETs based on various semiconductor materials also utilize double-gate structures for logic operations. The FeFET can adjust the polarization state of the ferroelectric gate dielectrics through the back gate. Different polarization states correspond to different logic input states, and the conversion of the logic gate can be realized by tuning the bias voltage of the top gate. The FGFET involves upper and lower gate structures on the gate dielectric, enabling the implementation of AND logic gates. By utilizing electrical inputs for Boolean logic operations, it is a widely adopted approach to construct a dual-gate structure capable of processing two logic inputs simultaneously.

6. Boolean Logic Operations Based on Optical Input: Photonic Boolean Logic

Most of the above-mentioned neuromorphic transistors use electrical stimulation as the Boolean logic input, which requires two or even three gate electrodes. However, electrical signals are not optimal in simulating human perception of external environmental stimuli. In contrast, optical neuromorphic transistors designed for light stimulation can replicate the human perception process, while also enabling multiterminal input without requiring additional electrodes. This allows for device miniaturization and faster response times.[23,114] Hence, utilizing light signals for Boolean logic calculations offers distinct advantages over electrical stimulation. Also, the optical neuromorphic transistor can be modulated by combining additional electrical stimulation to broaden the sensation fashion of the device.[60,68]

6.1. Electrical Modulation for Photonic Boolean Logic

The AND and OR logic gates can be realized through dendrites integrating two optical inputs and an electrically modulated signal (**Figure 8**a) and utilizing nanomaterials for the optical inputs offers several advantages due to their unique optical properties. 0D materials have light-absorbing capabilities from ultraviolet to near-infrared spectrum, while 2D materials have limited light absorption due to their ultra-thin structures.[115–116] Yin et al. fabricate optical neuromorphic transistors using boron-doped silicon nanocrystals (Figure 8b).[50] Light and electrical stimuli is introduced from the top and back gate of the device, respectively, to regulate synaptic plasticity by tuning the state of channel conductance. Inhibitory postsynaptic current (IPSC) can be triggered by applying 1342 nm wavelength light stimulation on the top gate and -50 mV electrical stimulation on the back gate, while the EPSC can be induced by applying 50 mV electrical trigger on the back gate. This behavior simulates the depolarization and repolarization process of the membrane potential in neuronal cells. In the application of Boolean logic, the two optical stimuli are used as the input terminals of the logic, and the electrical stimulation is used as the modulation terminal of the logic. The amplitude variation of IPSC is regarded as the output signal of the logic (10 pA as the threshold value). Corresponding results are shown in Figure 8c,d. An applied positive bias electrical stimulation induces EPSC to inhibit the initially induced IPSC by light pulse, which leads to the overall amplitude of IPSC to be small (this is an AND logic gate). In contrast, a negative electrical stimulation causes a larger change in the IPSC (this is an OR logic gate). The optical logic input can directly reduce the number of device gates, and the coupling with electrical stimulation can further broaden the logic operation modes.

TMDs have been demonstrated with excellent optoelectronic properties. Zhang et al. use monolayer MoS_2 as the semiconductor channel and $Pb(Zr_{1-x}Ti_x)O_3$ (PZT) as the ferroelectric dielectric layer to construct the photonic-memristive system (PMS) (Figure 8e).[117] Under light stimulation, the photogenerated carriers produced in MoS_2 accumulate at the interface between the semiconductor channel and the dielectric layer, thereby influencing the polarization field of PZT. Upon removal of light, the device transitions from the low resistance state (LRS) to the high resistance state (HRS). When the light stimulation is applied again, the device recovers from HRS to LRS and changes the polarization direction of PZT to adjust the channel conductance. In addition to photogenerated carriers, a higher source-drain voltage also generates a larger channel current and leads the PZT to be strongly polarized downward. At this moment, the device turns into the HRS allowing multilevel storage. As shown in Figure 8f, the Boolean logic operations are performed by connecting two MoS_2/PZT PMS in series with a 1 GΩ load resistor. The device is first brought into the initial HRS by using optical modulation. Two independent optical stimuli ($P_{In,A}$ and $P_{In,B}$) are used as the logic inputs, and the output voltage at the load is used as the logic output. This allows the operation of an AND logic gate (Figure 8g). Furthermore, the data can be stored for a relatively long time thanks to the storage properties of FeFET.

6.2. Optical Modulation for Photonic Boolean Logic

Figure 9a shows multiple logic gates of AND, OR, NAND, NOR, and XOR realized through dendrites integrating two optical inputs and one optical modulation signal. The use of light as the input and modulation signal is advantageous in terms of fast transmission speed, high bandwidth, and the ability to resist interference and crosstalk. Ahmed et al. construct an optical neuromorphic transistor using defective black phosphorus (BP) (Figure 9b).[118] Semiconducting BP has direct band gaps and high hole mobility, which enables detecting the spectral range from deep ultraviolet to infrared.[119–120] The induced defects during spontaneous oxidation of BP can result in unique optoelectronic properties.[121–123] The dissociation of ambient oxygen molecules on the surface of BP creates localized charge-trapping sites, resulting in a negative photocurrent when exposed to 365 nm light irradiation. This negative photocurrent can be effectively employed to emulate the IPSC in synaptic simulations. On the other hand, when exposed to 280 nm light, environmental hydrogen molecules split and passivate the oxygen sites, leading to a positive light response. This positive response is suitable for emulating the EPSC in synaptic simulations. Logical operations

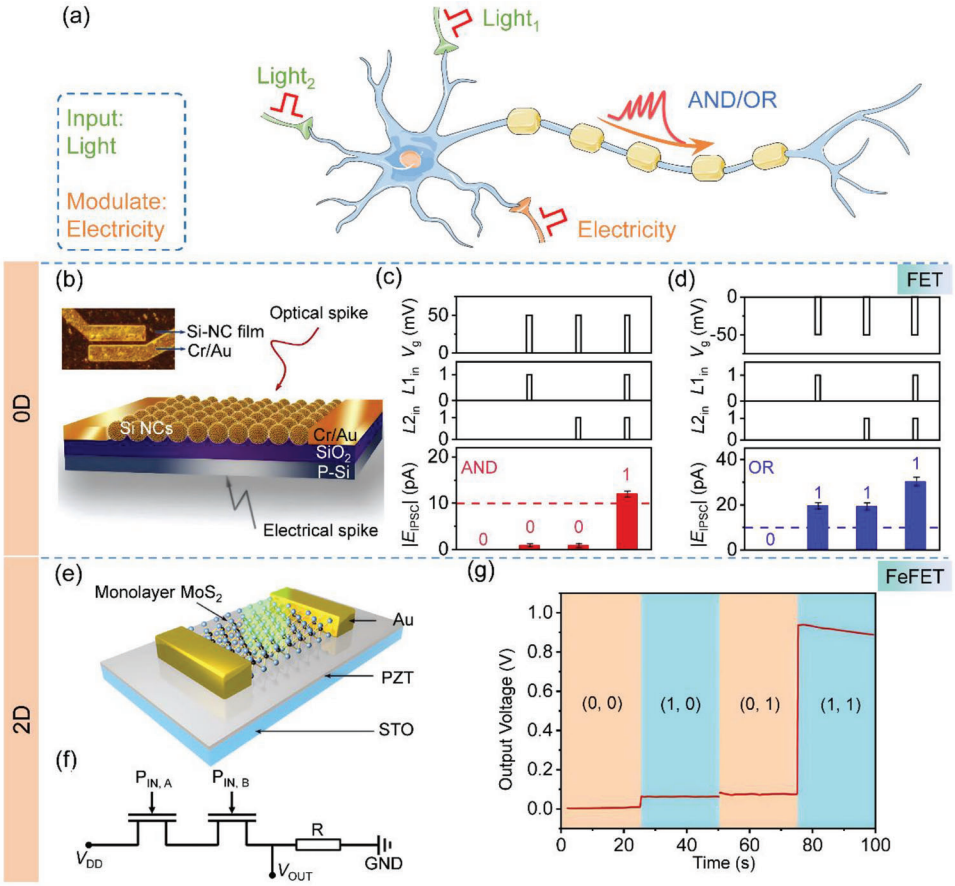

Figure 8. Boolean logic operations based on optical input and electrical modulation. a) Schematic diagram of neuron structure with dendrites integrating optical input and electrical modulation. b-d) Schematic diagram of optical neuromorphic transistors based on boron B doped silicon nanocrystals (Si NCs), and the input and output results of implementing Boolean logic through optical input and electrical modulation. Reproduced with permission.[50] Copyright 2019, Elsevier. This operation implements the conversion of AND and OR logic gates. e) Schematic diagram of the FeFET based on MoS_2 as the channel material and $Pb(Zr_{1-x}Ti_x)O_3$ (PZT) as the ferroelectric gate dielectric. f,g) Circuit diagrams based on connecting two MoS_2/PZT FeFETs in series with a 1 GΩ load resistor to perform Boolean logic operations, and the corresponding output results of Boolean logic operations. Reproduced with permission.[47] Copyright 2020, John WIley and Sons.

can be performed by connecting two BP neuromorphic transistors in series (device structure in Figure 9b). In their work, the authors use light inputs of A and B for two BP-based devices. Turning on/off the light corresponds to logical input "1"/"0", and the output current indicates the logic output. With Input A and Input B having wavelengths of 365 nm and 280 nm respectively, these two types of light induce the suppression and enhancement of the channel current, respectively. As single light irradiation can cause the change of the channel current individually, the suppression and enhancement of the channel current will be offset when the input light A and B are irradiated simultaneously. This case corresponds to an XOR logic gate whose resulting output is shown in Figure 9c. When the Input A and B have the same wavelength of 365 nm, the channel current changes as long as the light is irradiated (this is an OR logic gate, Figure 9d). Based on the positive and negative responses to different light irradiations through defect engineering, this work enriches the functions of BP devices and offers a new idea to the construction of new visual information processing and optoelectronic logic gates. Liang et al. fabricate a bidirectional photo-responsive device through $PtSe_{2-x}$ films synthesized by controllable selenization engineering (Figure 9e).[124] Due to the coupling between the positive photoconductivity effect of $PtSe_2$ and the negative radiative thermal effect of Pt, the photocurrent suppression and enhancement of the device are realized with light irradiation at 405 nm and 980 nm, respectively (i.e., IPSC and EPSC). Yang et al. construct a bidirectional photo-responsive device based on Bi_2O_2Se/graphene mixed structure (Figure 9f).[125] Light illumination at 365 nm and 635 nm decreases and increases the conductivity of the devices, respectively. In the Boolean logic operation, these devices use three input lights, two of which are for the basic inputs of the logic, and the other is for the modulation input of the logic. The logic output is shown in Figure 9g. As the light of 365 nm suppresses the photocurrent of Bi_2O_2Se/graphene, when it is used as the modulation signal, the logic output is less than the threshold of 2 μA at logic input "10" or "01" (this is an AND logic gate). When the 365 nm light is not applied, it yields an OR logic gate.

Metal oxide semiconductors (MOS) have high photosensitivity and charge-carrying capacity. This is because the light

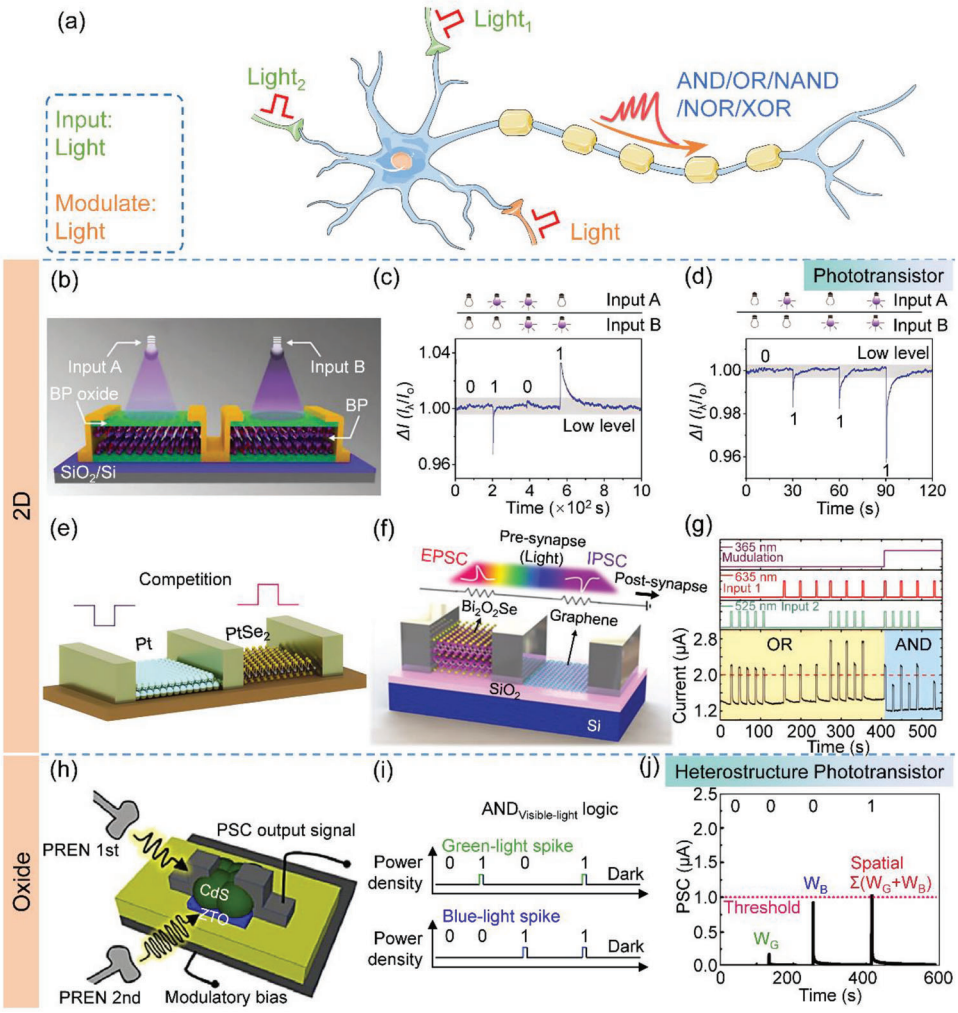

Figure 9. Boolean logic operations based on optical input and optical modulation. a) Schematic diagram of neuron structure with dendrites integrating optical input and optical modulation. b–d) Schematic diagram of the optical neuromorphic transistor constructed by the defective black phosphorus (BP), and the input and output results of Boolean logic are performed by optical input and optical modulation. This operation realizes the conversion between XOR and OR logic gates. Reproduced with permission.[119] Copyright 2017, Wiley. e) Schematic diagram of bidirectional photo-responsive neuromorphic transistors based on $PtSe_2$ and Pt. Reproduced with permission.[124] Copyright 2022, Wiley. f,g) Schematic diagram of a bidirectional photo-responsive neuromorphic transistor based on Bi_2O_2Se and graphene, and the input and output results of performing Boolean logic through optical input and optical modulation. This operation realizes the conversion between OR and AND logic gates. Reproduced with permission.[125] Copyright 2020, Wiley. h) Schematic diagram of optical neuromorphic transistors based on CdS and ZnSnO (ZTO) heterostructure. i,j) The input and output results of performing AND logic gate operations. Reproduced with permission.[33] Copyright 2019, Elsevier.

stimulation leads to oxygen vacancy ionization in MOS and the slow recovery results in long-term photoconductivity. The light stimulation can easily change the electrical properties of MOS-based neuromorphic transistors and can be used to update its synaptic weight.[10,126–127] Chao et al. construct a heterogeneous optical neuromorphic transistor through CdS and ZnSnO (ZTO) (Figure 9h).[33] Through the narrow band gap of CdS, the heterojunction can respond to a wider spectral range and improve the inefficient generation of the photoinduced charge carriers. In addition, the different crystallinity of CdS and ZTO Gives rise to a pronounced charge trap at the heterogeneous interface, which can reduce the recovery speed of photogenerated carriers, thus facilitating the emulation of synaptic behavior. In terms of Boolean logic, different logic operations can be performed by introducing light in different wavelengths. The on and off states of light can be defined as logical inputs "1" and "0". Corresponding input and output results of the AND logical operations are shown in Figure 9i,j. When the blue and green light is irradiated to the device, the output surpasses the threshold of 1 μA, implementing the logic operation. Notably, the logic output of the device exceeds the threshold even when ultraviolet light is irradiated.

Organic optical neuromorphic transistors use light-sensitive materials to improve the light response range. Zhang et al. construct an optical neuromorphic transistor using GDY and graphene as the active heterostructure channel and octadecyltrimethoxysilane (OTMS) as the hydrophobic modification layer (**Figure 10**a).[32] GDY film acts as a photo-responsive charge-trapping layer because of its excellent light absorption and

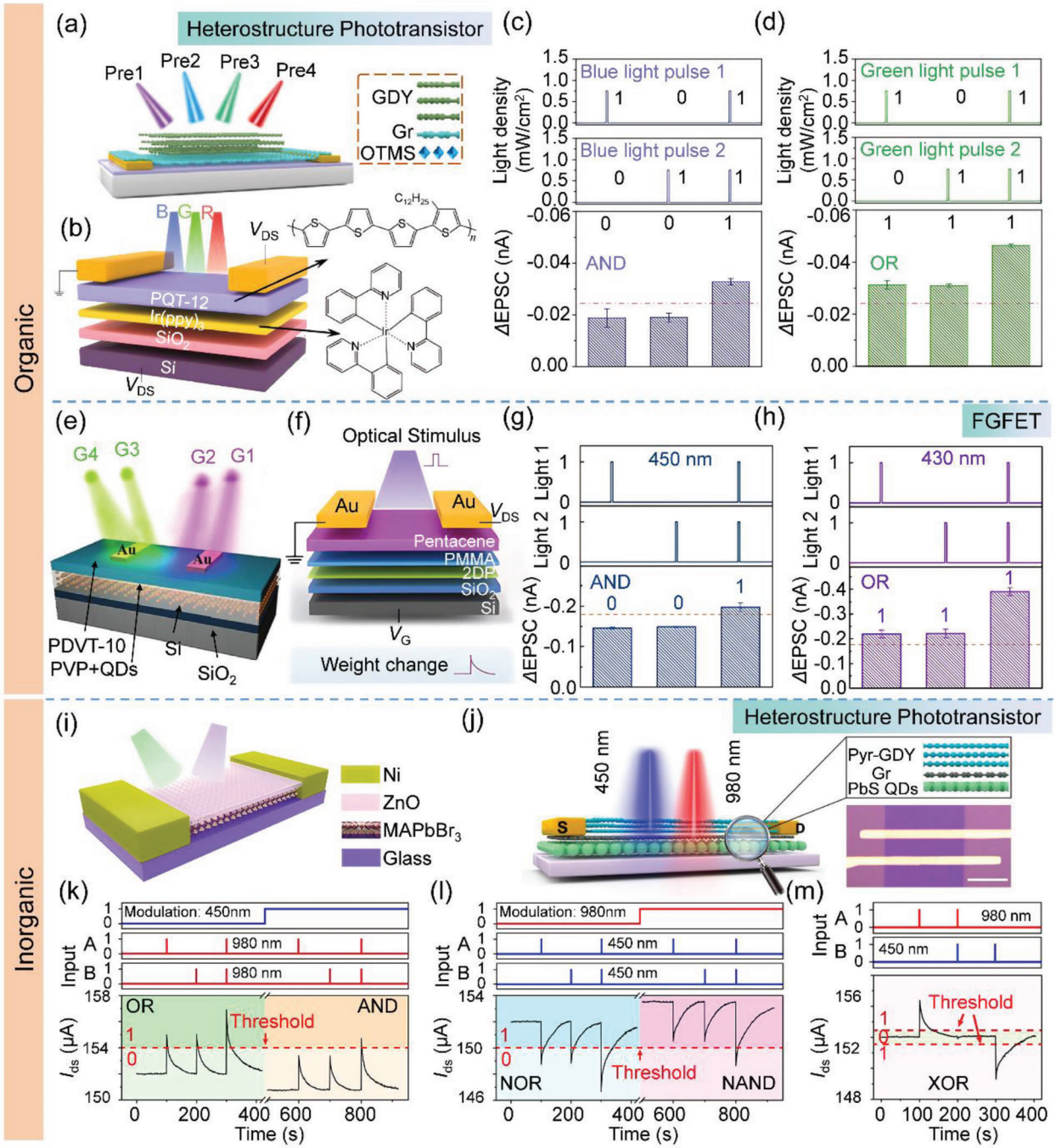

Figure 10. Boolean logic operations based on optical input and optical modulation. a) Schematic diagram of an optical neuromorphic transistor constructed based on GDY and graphene heterostructure with organic octadecyltrimethoxysilane (OTMS) layer as the hydrophobic layer. Reproduced with permission.[132] Copyright 2021, Springer Nature. b–d) Schematic diagram of the optical neuromorphic transistor based on Ttris(2-phenylpyridine) iridium (Ir(ppy)3) and poly(3,3-didodecylquarterthiophene) (PQT-12) organic heterojunction, and input and output results of Boolean logic operations performed through optical input and optical modulation. This operation implements the conversion of AND and OR logic gates. Reproduced with permission.[133] Copyright 2021, John Wiley and Sons. e) Schematic diagram of the optical neuromorphic transistor constructed based on PVP mixed with $CsPbBr_3$ QDs as the floating gate layer and PDVT-10 as the active layer. f) Schematic diagram of an optical neuromorphic transistor constructed based on two-dimensional imine polymers (2DPs) as the floating gate, PMMA as the gate dielectric, and pentacene as the active layer. g,h) The input and output results of Boolean logic operations are performed through optical input and optical modulation. This operation realizes the conversion between AND and OR logic gates. i) Schematic diagram of optical neuromorphic transistor based on perovskite single crystal $MAPbBr_3$ and ZnO heterostructure. Reproduced with permission.[134] Copyright 2022, WIley. j–l) Schematic diagram of optical neuromorphic transistor based on pyrene-based graphdiyne/graphene/PbS quantum dots (Pyr-GDY/Gr/PbS-QD) vertical heterogeneity, and the input and output result to perform Boolean logic operations through light input and light modulation. This operation implements four logic gates of AND, OR, NAND, and NOR. m) The input and output results of the XOR logic gate are realized by two different optical inputs, and the change of the channel current is set as the threshold.

charge-trapping ability.[128] OTMS can modify the surface of SiO_2 substrates, prevent the formation of Si-OH groups to inhibit the adsorption of H_2O molecules, and improve the charge carrier mobility of organic semiconductors.[129] In the application of Boolean logic based on the IPSC by light irradiation, the NAND logic gate can be realized when the red and green light is used as logic inputs, while the NOR logic gate can be realized by using ultraviolet light and blue light as logic inputs. Zhang et al. construct an organic optical neuromorphic transistor with tris(2-phenylpyridine) iridium (Ir(ppy)3) and poly(3,3-didodecylquarterthiophene) (PQT-12) heterostructure (Figure 10b).[130] Light stimulation is used as presynaptic input and the heterojunction channel is considered as the postsynaptic output. PQT-12 has a high response to visible light, while Ir(ppy)3 can be used as an electron trapping layer because of its high efficiency of electrophosphorescence.[23,131] Therefore, the organic heterostructure can regulate the electrical conductivity by light stimulation and regulate the synaptic plasticity. In the application of Boolean logic, light signals with different wavelengths are used as the logic inputs. A threshold of 0.025 nA is established to identify the logic output based on the variation of EPSC. The logic output is shown in Figure 10c,d. When the blue light is employed as the logic input, the device functions as an AND logic gate. Conversely, when the green light is utilized as the logic input, it operates as an OR logic gate. Aside from organic heterostructures, some studies have employed an organic channel combined with a charge-trapping layer to construct a FGFET. In this configuration, the slow de-trapping capability of the floating gate layer can be utilized to emulate synaptic behaviors. For instance, He et al. construct multi-input optical neuromorphic transistor using Polyvinylpyrrolidone (PVP) mixed with $CsPbBr_3$ QDs as the floating gate and PDVT-10 as the active semiconductor (Figure 10e).[34] The floating gate acts as the modulation layer to update the synaptic weight, and the PDVT-10 forms a conductive channel between the electrodes. The light irradiation in the wavelength of 500 and 400 nm is taken as the logic inputs, successfully realizing the conversion between AND and OR logic gates. Zhang et al. construct an optical neuromorphic transistor based on two-dimensional imide polymer (2DPs) as the floating gate, PMMA as gate dielectrics, and pentacene as the active layer (Figure 10f).[132] 2DPs can be used as a charge-trapping layer because of their unique band structure and tunable photophysical properties, and the 2DP floating gate can capture and store photogenerated carriers to modulate channel conductance. In addition, the high photosensitivity of 2DPs enables the device to exhibit synaptic characteristics at a low operating voltage of 0.1 V. For Boolean logic operation, this work also uses different light as logic input. The EPSC change of 0.18 nA is set as the threshold for the logical outputs. The light stimulation in the wavelength of 450 nm and 430 nm is used as the logic inputs to implement the conversion of AND and OR logic gates (Figure 10g,h).

In addition to organic heterostructures, inorganic heterostructures can also be used in high-performance optoelectronic devices and flexible photonic artificial synapses.[12,133] The most important bidirectional photo-responsive neuromorphic transistors built through heterostructures can realize multiple Boolean logic operations through a single device. Ge et al. adopt a heterostructure of perovskite single-crystal $MAPbBr_3$ and ZnO to construct an optical neuromorphic transistor (Figure 10i).[134] This device possesses several advantages; single crystal $MAPbBr_3$ has the advantages of high absorption coefficient, fast carrier mobility, and low trap density while ZnO allows desorption of chemisorbed oxygen ions from the surface upon UV irradiation, resulting in an increase in conductivity. The slow recovery of current in the device following the removal of light exposure offers significant advantages in mimicking synaptic function.[135–136] The heterostructure of ZnO and $MAPbBr_3$ is beneficial to the construction of high-performance optoelectronic transistors. Lastly, the heterogeneous device has bidirectional photo-responsive properties allowing EPSC and IPSC characteristics: under the irradiation of UV and green light, the channel current is enhanced and suppressed, respectively. This feature can be utilized to demonstrate the operation of Boolean logic. When two 365 nm lasers are used as the logic input terminals and the 520 nm light is used as the logic modulation terminal, an AND logic gate can be achieved when the green light is on, and an OR logic gate can be implemented when the green light is off. However, when two 520 nm lasers are used as the logic input terminals and the 365 nm light is used as the logic modulation terminal, NAND logic gates can be realized when UV light is turned on, and NOR logic gates can be realized when UV light is turned off. In this fashion, four Boolean logic operations are successfully realized through bidirectional photo-responsive heterojunctions.

Similarly, Hou et al. construct an optical neuromorphic transistor with vertical heterostructures of pyrene-based graphdiyne/graphene/PbS quantum dots (Pyr-GDY/Gr/PbS-QD) (Figure 10j).[137] The photogenerated carriers in Pyr-GDY and PbS-QD can induce inhibitory and excitatory synaptic properties and linearly regulate the conductance of graphene. The bidirectional photo-response of the device produces IPSC and EPSC characteristics under 450 nm and 980 nm light, respectively. Accordingly, it is also possible to implement four kinds of logic gates: AND, OR, NAND, and NOR. The relevant logical input and output results are presented in Figure 10k,l. When the device is irradiated to 980 nm light (the logic input), the 450 nm light is used as the modulating parameter for the logic. AND logic gate can be realized when the 450 nm is turned on, while the OR logic gate can be realized when the green light is turned off. In contrast, when the device is irradiated to 450 nm light (the logic input), the 980 nm light is used as the modulation input for the logic. In this case, the NAND logic gate can be realized when the 980 nm light is turned on, while the NOR logic gate can be realized when the 980 nm is turned off. For the XOR logic gate (Figure 10m), the simultaneous irradiation of light in two different wavelengths causes the counteraction of EPSC and IPSC due to the characteristics of the bidirectional photo-response, yielding a logical output of "0". When different light is irradiated independently, the logical output result "1" is achieved.

6.3. Section Summary

In **Table 2**, we summarize the Boolean logic operations implemented in optical neuromorphic transistors. Optical signal has the ability of fast transmission speed, broad bandwidth, anti-interference, and anti-crosstalk, exhibiting great advantages in Boolean logic operation. Compared to the Boolean logic operations by electrical inputs which generally require multigate

Table 2. Boolean logic operations based on optical input.

Modulation strategy	Type	Device structure	Channel materials	Gate dielectric	Logic	Ref.
Electricity	0D	FET	Si NCs	SiO_2	AND/OR	[50]
	2D	FeFET	MoS_2	PZT	AND	[117]
Light	2D	Phototransistor	BP	SiO_2	XOR/OR	[118]
		Phototransistor	Bi_2O_2Se, Graphene	SiO_2	AND/OR	[125]
		Phototransistor	$PtSe_2$, Pt	\	AND/OR	[124]
	Oxide	Heterostructure Phototransistor	CdS/ZTO	SiO_x	AND	[33]
	Organic	Heterostructure FET	PQT-12/$Ir(ppy)_3$	SiO_2	AND/OR	[130]
		Heterostructure FET	GDY/GR /OTMs	\	NAND /NOR	[32]
		FGFET	Pentacene	2D polymers	AND/OR	[132]
		FGFET	PDVT-10	PVP/$CsPbBr_3$	AND/OR	[34]
	Inorganic	Heterostructure Phototransistor	$MAPbBr_3$	ZnO	AND/OR	[134]
		Heterostructure Phototransistor	Pyr-GDY/Gr /PbS-QD	\	AND/OR/NAND/NOR/XOR	[137]

architectures, the optical input can greatly simplify the fabrication process. Besides, the optical signal can be coupled with the electrical signal for synergistic logical operation. The positive and negative bias of the electrical signal can have different effects on the conductance of the device, inducing EPSC (or IPSC) to enhance (or inhibit) the postsynaptic current induced by light stimulation. In general, the enhanced postsynaptic currents can be used for OR logic gate, while the inhibitory postsynaptic currents can be used for AND logic gate. For FeFET, the gate near the ferroelectric side can preset the polarization direction in the ferroelectric dielectrics and adjust the channel conductance so that the device can be tuned between HRS and LRS. Devices that utilize optical modulation typically exhibit bidirectional photo-response characteristics, wherein the light of a specific wavelength can induce EPSC, while light of another wavelength can trigger IPSC. For example, BP with defects can cause IPSC and EPSC under light illumination at 405 and 980 nm, respectively. However, most devices based on a single active layer do not have the property of bidirectional photo-response, limiting its applications that involves complex Boolean logic operations. By conjugating two types of active materials, coplanar series structures or heterojunctions can be utilized to address this issue and construct optical neuromorphic transistors. For example, the coupling between positive conductance effect of $PtSe_2$ and negative radiation thermal effect of Pt can induce IPSC and EPSC when the device is irradiated at 405 and 980 nm, respectively. The heterostructures of $MAPbBr_3$ and ZnO can cause EPSC and IPSC when the green and UV light is irradiated, respectively. The bidirectional photo-responsive devices can implement various Boolean logic gates. By using a light with a certain wavelength as the logic inputs and other light in different wavelengths as the modulation input, AND, OR, NAND, and NOR logic gates can be realized. When two distinct types of light are utilized as the logic inputs in the absence of modulation of the optical signal, it is possible to synergistically modulate the enhancement and suppression of the postsynaptic current, allowing the realization of more complex XOR logic gates. In addition, organic neuromorphic transistors induce different gain effects in EPSC when stimulated by different wavelengths of light. The devices with large postsynaptic current variations can be used for OR logic operations, while those devices with small variations can be used for AND logic operations. In summary, the devices based on optical input can achieve various Boolean logic, which is of great significance for the construction of future neuromorphic computation with multifunctionality, high computational efficiency, and high integration capacity.

7. Boolean Logic Operations Based on Synergistic Optical/Electrical Input: Photo-Electronic Boolean Logic

The Boolean logic operations discussed above mainly adopt single signal input mode (either electrical input or optical input). In this section, the Boolean logic devices are discussed by utilizing two types of logic inputs (synergistic electrical input together with optical input). Corresponding Boolean logic conversions are realized by using electrical or optical signals as the modulation input, so as to realize dynamic programmable logic functions.

7.1. Synergistic Optical/Electrical Inputs For Boolean Logic Operations

AND and OR logic gates can be realized through dendrites integrating synergistic optical/electrical signals as two logic inputs and an individual electrical or optical signal as the modulation input (**Figure 11**a). The reported synergistic optical/electrical logic devices are mostly based on low-dimensional materials, which have high electron mobility and PPC effect under light stimulation.[16,138] In addition, 2D materials can form heterostructures with other systems of materials to achieve unique interfacial charge transport properties, which is beneficial for the construction of various types of optoelectronic devices and neuromorphic computing.[139–140]

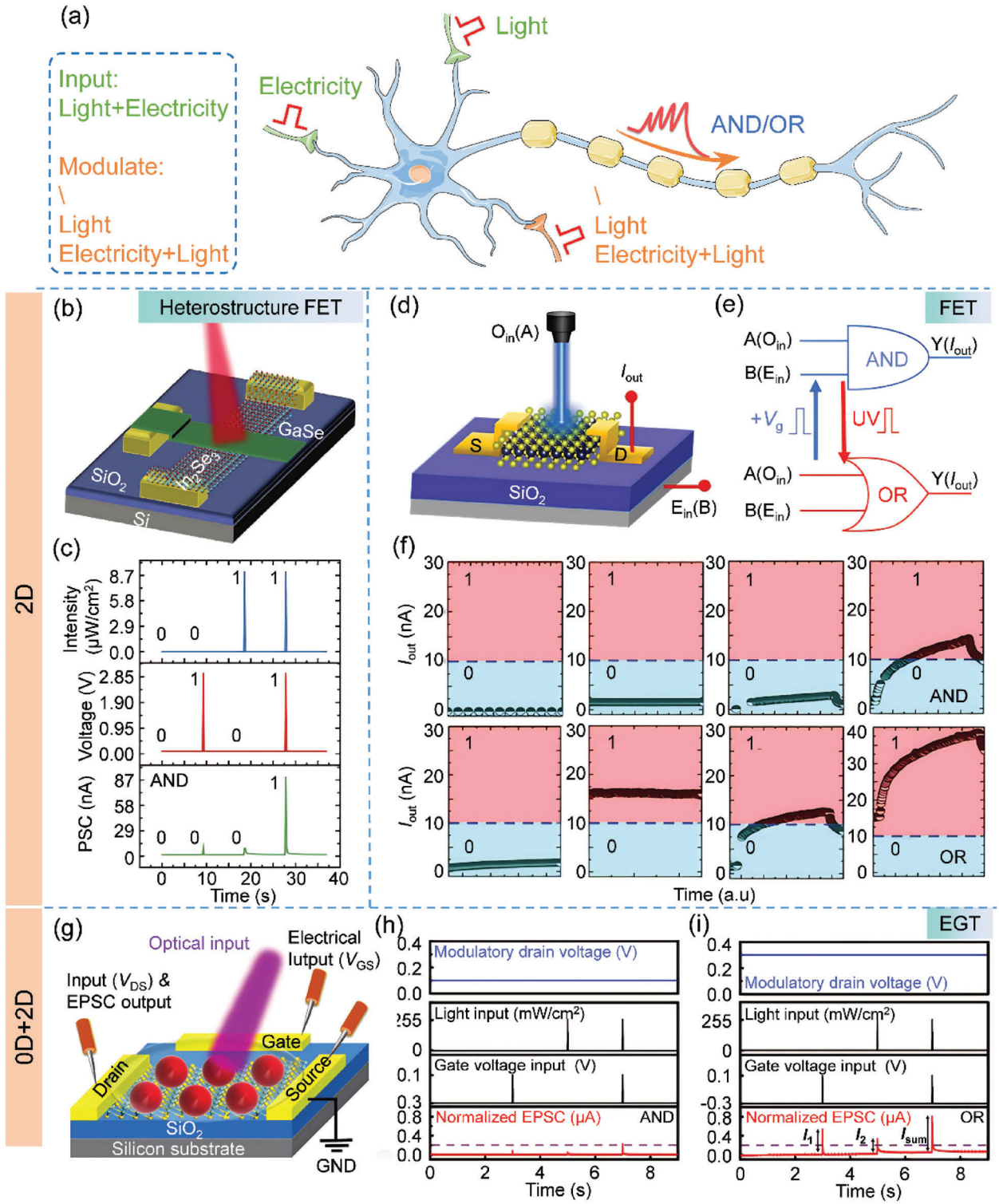

Figure 11. Boolean logic operation based on synergistic optical/electrical input. a) Schematic diagram of neuron structure with dendrites integrating optoelectronic inputs, and the modulation terminal can be an optical signal or an electrical signal. b,c) Schematic diagram of optoelectronic neuromorphic transistor based on α-In_2Se_3 and GaSe heterostructures, and the input and output results of AND logic gates based on optoelectronic input. Reproduced with permission.[32] Copyright 2021, Wiley. d) Schematic diagram of optoelectronic neuromorphic transistors based on monolayer MoS_2. e,f) Flow chart and output result of performing Boolean logic gate conversion based on optical signal and electrical signal modulation. After pre-irradiation through the UV of 390 nm, the OR logic gate can be realized. Through the gate bias of 30 V, the AND logic gate can be realized. Reproduced with permission.[52] Copyright 2022, Wiley. g) Schematic diagram of EGT based on $CsPbBr_3$ QDs and MoS_2 heterojunction. h,i) The input and output results of Boolean logic operations through optoelectronic input and electrical modulation. This operation realizes the conversion between AND and OR logic gates.

Table 3. Boolean logic operations based on synergistic optical and electrical inputs.

Modulation strategy	Type	Device structure	Channel materials	Gate dielectric	Logic	Ref.
\	2D	Heterostructure FET	α-In_2Se_3/GaSe	SiO_2	AND	[51]
Electricity+Light		FET	MoS_2	SiO_2	AND/OR	[52]
	0D+2D	EGT	$CsPbBr_3$ QDs/MoS_2	Ion-gel electrolyte	AND/OR	[29]

Guo et al. build an optoelectronic neuromorphic transistor through the heterostructure of n-type ferroelectric α-In_2Se_3 and p-type GaSe (Figure 11b).[51] α-In_2Se_3 has a narrow bandgap of 1.4 eV, and its ferroelectricity can enrich the functionalization of the device and enhance the information processing ability. In the application of Boolean logic, a combination of synergistic electrical signals and optical signals is employed as the logic inputs. The optical signals correspond to logic inputs "1" (light turned on) or "0" (light turned off). For electrical signals, a bias of 3 V is applied for logic input "1" and a bias of 0.1 V is applied for logic input "0". The logic input and output results are shown in Figure 11c, demonstrating an AND logic operation. Furthermore, a large difference in the PSCs caused by the separate input or synergistic inputs of electrical and optical signals can contribute to enhancing the accuracy of logic operations.

Sahu et al. use monolayer MoS_2 to construct an optoelectronic neuromorphic transistor (Figure 11d).[52] Both the light and electrical pulses can regulate the conductance of MoS_2 channels to update the synaptic weights. In terms of Boolean logic operations, turning on and off the blue light is utilized as the logic input of "1" and "0", respectively. For electrical signals, the gate is unbiased for logic input "1", and a bias of −20 V is applied for logic input "0". By setting 10 nA as the threshold for logic output, neither the intrinsic electrons nor the photogenerated carriers in the channel can induce the output to exceed the threshold, implementing an AND logic operation. However, after preirradiation with 390 nm UV, the PPC effect of the device can be significantly improved. OR logic gates can be implemented by using the same blue light and electrical pulses as the logic inputs. By applying a gate bias of 30 V, the device exhibits a conductance state that enables the initial AND logic operation. In this fashion, the synergistic UV and electrical stimuli can modulate the conductance of the channel and realize the conversion between OR and AND logic gates (Figure 11e). Corresponding logic outputs are shown in Figure 11f.

Cheng et al. construct an optoelectronic neuromorphic transistor by using the heterojunction of 0D $CsPbBr_3$ QDs and 2D MoS_2 as the channel material and the polymer ion gel electrolyte (PIGE) as the gate dielectrics (Figure 11g).[29] 0D QDs have a high light absorption coefficient, and 2D materials have high carrier mobility. The combination of the two materials can significantly improve the device performance. The EDL characteristics of PIGE allows simulating of the dynamic properties of biological synapses, and the PIGE can also prevent channel materials from being oxidized. In terms of Boolean logic applications, the device has exhibited a variety of feasible Boolean logic input/modulation strategies. When the drain voltage and the optical signal are used as two logic inputs, the gate voltage can be used as the modulation signal to realize the AND logic gate. When the gate voltage and the optical signal are used as two logic inputs, the drain voltage can work as the modulation signal to realize the conversion between AND and OR logic gates. Available logic input strategies and corresponding logic output results are shown in Figure 11h,i.

7.2. Section Summary

In **Table 3**, we summarize the Boolean logic operations based on synergistic optical/electrical inputs. Most of these devices use low-dimensional materials with excellent optical absorptivity and carrier migration velocity to construct optoelectronic neuromorphic transistors. Synergisticoptical/electrical signal input/modulation can lead to demanded Boolean logic functions. The optical and electrical signals are used as the logic inputs, and the modulation method includes either optical or electrical modulation. For example, single-layer MoS_2 devices can be used to implement OR logic operation through UV pretreatment, while the AND logic gates can be realized after electrical signal processing. The conversion of different logic gates can also be realized through the synergistic optical/electrical modulation. However, research on tunable Boolean logic operations based on optoelectronic neuromorphic transistors remains limited, highlighting the pressing need for the development of more sophisticated devices.

8. Summary and Perspective

This paper reviews Boolean logic computing based on neuromorphic transistors. The logic operations are primarily relying on CMOS logic circuits and dendritic integration. In **Figure 12**, we summarize the advantages and challenges of Boolean logic operations associated with dendritic integration. The neuromorphic transistors can adjust the synaptic weight through multiple input signals in a single device and then integrate them to implement Boolean logic operations. In addition, this operation mode effectively avoids the need for complex wiring and a multitude of transistors that are typically required in traditional CMOS logic circuits. This aspect holds significant importance in the construction of artificial neural networks with high integration density and computational efficiency for future applications. Neuromorphic transistors have also exhibited multiple input strategies to implement Boolean logic operations, which is systematically summarized and categorized into electrical input, optical input, and synergistic optical and electrical input in this review. Besides, more sophisticated logic functions can be programmed by (tribo)electrical, optical, and thermal modulations.

Up until now, there have been several challenges in the research of Boolean logic computing based on neuromorphic

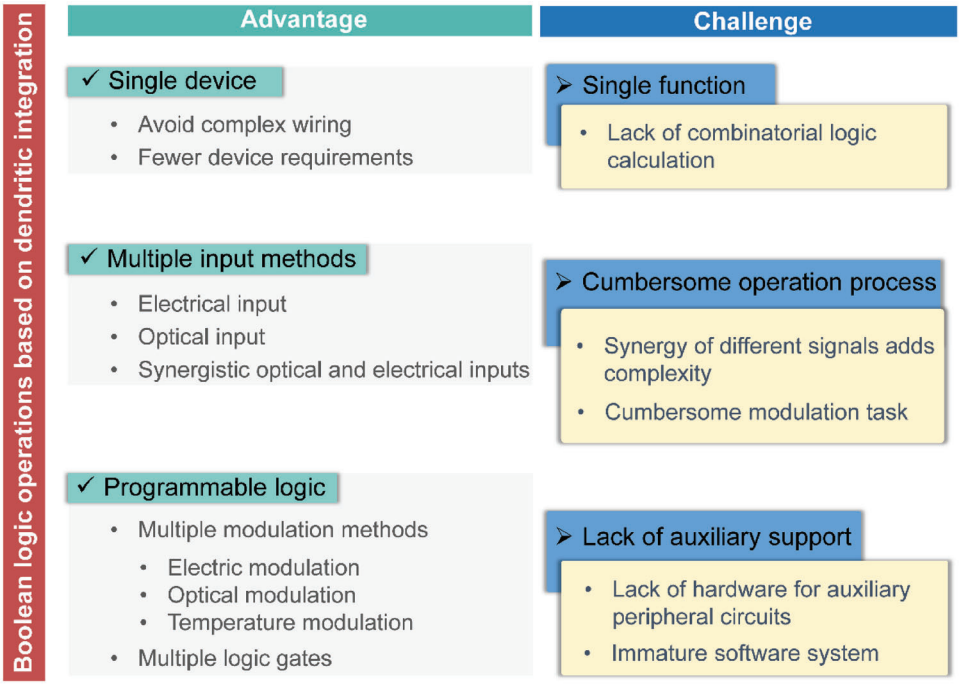

Figure 12. Advantages and challenges of Boolean logic operations based on dendritic integration.

transistors. First, one major limitation is that most of the research focus only on realizing of basic logic functions, lacking in combined logic calculation and functionalization. For instance, most devices only implement AND and OR logic gates, with few demonstrating the combined functions formed by these two logic gates. Therefore, further implementation of other logic gates (e.g., XOR) and more complicated logic circuits is desired. The combination of XOR logic gates with AND and OR logic gates is crucial for performing digital calculations as it enables the creation of adders and multipliers. In general logic circuits, XOR logic gates are constructed by combining NOT, AND, and OR logic gates. In contrast, the bidirectionally responsive neuromorphic transistors can be readily used to implement XOR logic gates. In particular, when two logic inputs cause the excitation and inhibition of PSC, the mutual cancellation of the excitatory and inhibitory effects can realize the XOR logic gate through linear integration. Therefore, the development of bidirectional responsive neuromorphic transistors is expected to become a prominent trend in the field of neuromorphic computing, significantly enhancing device functionalization.

Second, the process of performing Boolean logic operations in neuromorphic transistors can be cumbersome. The synergy of different signals adds complexity to the process, and optical signals require the support of additional light sources. The conversion of logic gates often requires additional modulating signals to ensure consistent operation with the input signals. However, this process of modulation causes complexity and increase in power consumption. In other words, the more signals that need to be processed for Boolean logic operations by dendritic integration, the more complex process becomes.

Third, the emerging neuromorphic transistors currently lack paired supporting strategies. Unlike well-established traditional computing architectures, research on neuromorphic transistors has primarily focused on implementing basic logic gates. These gates are typically controlled by mechanical switches, which results in slower operation compared to general CMOS logic circuits. In this context, the development of neuromorphic transistors requires paired support circuits for signal emission, signal reading, and controllers to improve logic gate operation. As the addition of auxiliary peripheral circuits are introduced, the number of components inevitably increases. In addition to hardware, the immature software systems can also limit the development of neuromorphic transistors.

Currently, the state of neuromorphic transistor technology is still in its early stage and has some limitations compared to CMOS technology. Challenges in terms of manufacturing complexity, reliability, and integration need to be addressed. Therefore, achieving widespread application of neuromorphic transistors and completely replacing CMOS technology still faces big technological challenges. To fully exploit the advantages of both technologies, one possible approach is to integrate neuromorphic transistors and CMOS circuits on the same chip. The CMOS component can be used to deal with logical computation, control, and transmission, while the neuromorphic transistors can perform tasks such as simulating neural networks, neuromorphic computation, and pattern recognition. The integration of neuromorphic transistors and CMOS enables computer systems to have both traditional sequential computing capabilities and the parallel processing capabilities of neuromorphic computation, thereby providing higher efficiency and flexibility in handling various tasks. The mixed integration approach can be considered as a transitional method towards the next generation of computing systems, which is established based on current technological achievements. Although there are still some challenges associated with implementing Boolean logic operation based on neuromorphic transistors, the exploration and

implementation of neuromorphic computing with high efficiency and high integration density are intensively investigated as one of the most promising mainstreams for future computation architecture and paradigm.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

Boolean logic, dendritic integration, neuromorphic transistor, programmable logic, Von Neumann architecture

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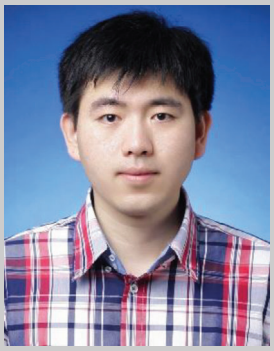

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